UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF TEXAS
WACO DIVISION

PARKERVISION, INC.,
Plaintiff,

vs.

INTEL CORPORATION,
Defendant.

Civil Action No. 6:20-cv-00108-ADA

JURY TRIAL DEMANDED

[redacted]

PUBLIC VERSION

DEFENDANT INTEL CORPORATION'S MOTION TO EXCLUDE OPINIONS AND TESTIMONY FROM PLAINTIFF'S TECHNICAL EXPERT DR. MICHAEL STEER

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I. INTRODUCTION

Intel respectfully moves to exclude opinions from ParkerVision's technical expert Michael Steer related to (1) the alleged conception, reduction to practice, and diligence (collectively, "C/RTP") for certain asserted claims; and (2) alleged infringement based on purported circuit-level simulations of the Intel products-at-issue.

First, Dr. Steer's opinions on ParkerVision's alleged conception and reduction to practice for asserted claim 5 of the '902 patent, claim 6 of the '725 patent, and claims 5 and 17 of the '673 patent should be excluded because Dr. Steer relies on a new C/RTP theory and more than 1,000 documents that ParkerVision never identified during fact discovery as allegedly relevant to C/RTP.[1] Dr. Steer's untimely reliance on this theory and evidence violates the Federal Rules and significantly prejudices Intel; his opinions should be excluded for this reason alone. In addition, Dr. Steer's C/RTP opinions are inadmissible as unreliable under *Daubert v. Merrell Dow Pharmaceuticals, Inc.*, 509 U.S. 579 (1993), and Federal Rule of Evidence 702 because Dr. Steer has failed to apply the Court's claim construction for the "storage element" limitations, and has applied no methodology whatsoever—much less a reliable methodology as required under *Daubert* and FRE 702—to show that ParkerVision's alleged embodiment of the invention practiced the "storage element" limitations.

Second, Dr. Steer's infringement opinions based on his circuit-level simulations of Intel's products should be excluded under *Daubert* and FRE 702 because he did not reliably apply standard circuit-simulation methodology. Dr. Steer's circuit-level simulations are based on inexplicably inaccurate assumptions about Intel's products: Dr. Steer simulated the Intel products using an ***ideal*** switch (which is not actually included in any of the Intel products) rather than a

[1] The "'902 patent" is U.S. Patent No. 6,580,902; the "'725 patent" is U.S. Patent No. 8,588,725; and the "'673 patent" is U.S. Patent No. 9,444,673. Emphases are added unless otherwise noted.

real-world transistor (which is included in the Intel products). Dr. Steer's methodological error is inexplicable because Dr. Steer ran other simulations using a real-world transistor model that he could have used in the circuit-level simulations on which he relied for his infringement analysis. As explained below, this fundamental methodological error and inconsistency in his methods had a significant impact on Dr. Steer's simulation results and make his infringement analysis unreliable and subject to exclusion under *Daubert* and FRE 702.

II. BACKGROUND

A. ParkerVision Failed To Disclose Its C/RTP Theory Or Evidence To Support An August 21, 1997 Invention Date During Fact Discovery.

Throughout discovery, Intel sought information on the C/RTP theory and evidence ParkerVision intends to rely on at trial. At the beginning of fact discovery, Intel served Interrogatory No. 2 asking ParkerVision to "identify and describe in detail all facts relevant to the conception and reduction to practice," including "the Date of conception" and "the Date of the first reduction to practice"; "all facts and circumstances Relating to any alleged diligence between the asserted conception and reduction to practice Dates"; and "the identity of all Documents (by Bates numbers) [r]elating to such conception, reduction to practice, and/or diligence." Ex. 1, Intel First Set of Interrogs. (Nos. 1-17) at No. 2 (Jan. 29, 2021).[2]

ParkerVision responded by listing "August 21, 1997" as the alleged "Priority Date" for asserted claim 5 of the '902 patent, claim 6 of the '725 patent, and claims 5 and 17 of the '673 patent—a date before the filing of the earliest relevant ParkerVision patent application. *See* Ex. 2, PV Suppl. Resp. to First Set of Interrogs. (June 21, 2022) at 5-9. ParkerVision, however, did not explain its C/RTP theory whatsoever; it provided no narrative explanation regarding its the alleged conception and reduction to practice. *Id.* Instead, ParkerVision only cited to documents:

[2] All exhibits are attached to the Declaration of Harry Hanson, filed concurrently herewith.

> Documents evidencing the conception, reduction to practice and/or diligence between the conception and reduction to practice of the asserted claims were produced along with ParkerVision's June 26, 2020 Preliminary Infringement Contentions. Pursuant to Fed. R. Civ. Pro. 33(d), ParkerVision identifies these documents as being responsive to this interrogatory.

Id. at 7. The referenced documents produced with ParkerVision's preliminary infringement contentions included, (1) excerpts from an expert report from a ParkerVision litigation with Qualcomm, which do not mention the '902, '725, or '673 patents at all much less explain a possible August 21, 1997 invention date (Ex. 3, PV_011945); (2) an evaluation report by The Boeing Company for ParkerVision's "Eddie" chip from 1998 (Ex. 4, PV_011928); (3) a test report from ParkerVision also dated 1998 (Ex. 5, PV_011950), and (4) high-level layout and graphical files (*e.g.*, Ex. 6, PV_011983).

ParkerVision also cited two prior interrogatory responses (which themselves cite to other documents) from ParkerVision litigations involving Qualcomm, in which the '902, '725, and '673 patents were not asserted. Ex. 2, PV Suppl. Resp. to First Set of Interrogs. (June 21, 2022) at 8 (ParkerVision identifying "Bates No. PV00415977 (Response to Rog. No. 3) and Ex. 9 (Response to Rog. No. 9) from the 1/27/2020 deposition of Cindy French as containing relevant information to this Interrogatory"). Neither cited response mentions the '902, '725, or '673 patent at all, and neither alleges—let alone shows—that any ParkerVision patent claim was entitled to an August 21, 1997 invention date. *See* Ex. 7, PV00415977 at 9-12; Ex. 8, French Dep. Ex. 9 at 33-41.[3]

[3] ParkerVision later supplemented its response to cite additional interrogatory responses from ParkerVision's litigations against Qualcomm: "Bates Nos. PV-REV0000001907 [*sic*] (response to Interrogatory Nos. 9, 10, 13) as containing relevant information to this Interrogatory." Ex. 2, PV Suppl. Resps. to First Set of Interrogs. (June 21, 2022) at 9. The cited interrogatory responses—which ParkerVision later clarified were produced at Bates no. PV_048170 (Ex. 9, Oct. 24, 2022 Email from Daignault)—again do not mention the '902, '725, or '673 patents, or allege that any ParkerVision patent claim was entitled to an August 1997 invention date. Ex. 10, PV_048170 at -178-182, -185-186.

In short, ParkerVision never advanced any theory or description of any August 21, 1997 alleged conception or reduction to practice for the asserted claims.

B. Intel Relied On ParkerVision's C/RTP Disclosures.

Intel relied on ParkerVision's responses to Interrogatory No. 2. ***First***, Intel questioned ParkerVision's 30(b)(6) witness on C/RTP based on ParkerVision's interrogatory response. When asked, ParkerVision's 30(b)(6) witness was unable to give the date or year when ParkerVision allegedly came up with the ideas that resulted in the asserted claims. *See* Ex. 11, Parker Dep. (June 22, 2022) at 33:16-35:4. And when shown ParkerVision's response to Interrogatory No. 2, ParkerVision's 30(b)(6) witness could not explain, or identify any document to support, ParkerVision's claimed August 21, 1997 invention date. *See* Ex. 27, Parker Dep. (June 23, 2022) at 598:3-602:25. That testimony is binding on ParkerVision. *Function Media, L.L.C. v. Google, Inc.*, 2010 WL 276093, at *1 (E.D. Tex. Jan. 15, 2010).

Second, Intel conducted its prior-art investigation and prepared its invalidity contentions based in part on ParkerVision's interrogatory responses, which did not set forth any theory or identify evidence to support an August 21, 1997 invention date.

Third, during expert discovery, Intel's technical expert Dr. Vivek Subramanian responded to the evidence set forth in ParkerVision's response to Interrogatory No. 2. Dr. Subramanian concluded that "the evidence that ParkerVision has presented in its interrogatory responses for earlier potential Invention Dates fails to show the necessary conception and diligent reduction to practice required to establish such dates." Ex. 12, Subramanian Opening Rpt., ¶204 (Aug. 29, 2022). To support that conclusion, Dr. Subramanian explained in detail why the documents ParkerVision produced with its preliminary infringement contentions in this case, ParkerVision's prior interrogatory responses from the Qualcomm litigations, and the documents ParkerVision cited in those prior interrogatory responses, were insufficient. *Id.*, ¶¶200-215. Dr. Subramanian

identified alternative invention/priority dates that were justified based on the evidence ParkerVision had identified (*id.*, ¶200), and his subsequent invalidity analysis was based, at least in part, on ParkerVision's failure to articulate any basis for an August 21, 1997 invention date.

C. Dr. Steer Advances A New C/RTP Theory And Newly Identified Documents In His Rebuttal Report.

Only after Intel's expert Dr. Subramanian had submitted his opening invalidity report did ParkerVision begin to allege a basis for an August 21, 1997 invention date—with an expert rebuttal report that relies on a new theory and documents that ParkerVision never before identified to Intel as relevant to C/RTP. ParkerVision's expert, Dr. Steer, still did not offer any narrative explanation of ParkerVision's alleged conception or reduction to practice in his report. *See* Ex. 13, Steer Rebuttal Rpt., ¶¶106-108. But he prepared claim charts that purport to map "documents evidencing early conception/priority of the asserted claims." *Id.*, ¶107; Ex. 14, Steer Rebuttal Rpt., Ex. D-1 ('902 patent chart); Ex. 15, Steer Rebuttal Rpt., Ex. D-3 ('725 patent chart); Ex. 16, Steer Rebuttal Rpt., Ex. D-6 ('673 patent chart).

Dr. Steer's rebuttal report charts disclosed, for the first time, a new ParkerVision theory that a circuit board schematic allegedly from August 1997—never cited previously by ParkerVision in its interrogatory responses—supports an August 21, 1997 invention date for claim 5 of the '902 patent, claim 6 of the '725 patent, and claims 5 and 17 of the '673 patent. Ex. 14, Steer Rebuttal Rpt., Ex. D-1 ('902 patent chart) at 5 ("The schematic of a circuit board with the Eddie-1 IC is dated August 21, 1997 and shown below."); Ex. 15, Steer Rebuttal Rpt., Ex. D-3 ('725 patent chart) at 5 (same); Ex. 16, Steer Rebuttal Rpt., Ex. D-6 ('673 patent chart) at 5 (same). Indeed, Dr. Steer's C/RTP analysis relies on ***more than 1,000 documents*** never cited in ParkerVision's response to Interrogatory No. 2: (1) an alleged August 21, 1997 ParkerVision circuit board schematic diagram and a related document that were never cited in ParkerVision's

interrogatory response (CONF-PV00175452; CONF-PV00175453); (2) a block diagram that Dr. Steer apparently prepared based on the alleged August 21, 1997 circuit board schematic that ParkerVision had not identified in its responses;[4] and (3) an Excel file that listed by Bates number and file name well over 1,000 documents—never previously identified to Intel as relevant to C/RTP—that Dr. Steer claims show ParkerVision's "diligen[ce]" in reducing the alleged inventions to practice. Ex. 13, Steer Rebuttal Rpt., ¶107; Ex. 19, Steer Rebuttal Rpt., Ex. D-7.

III. ARGUMENT

A. Dr. Steer's C/RTP Opinions Should Be Excluded.

i. Dr. Steer's C/RTP opinions should be excluded because ParkerVision failed to disclose its C/RTP theory and evidence during fact discovery.

Despite Intel's specific discovery requests, ParkerVision and its 30(b)(6) representative never disclosed during discovery: (1) any C/RTP theory to support an alleged August 21, 1997 invention date; or (2) the ***more than 1,000 documents*** that Dr. Steer now relies on in his C/RTP analysis. These failures blatantly violate Rule 26, prejudice Intel, and should preclude Dr. Steer from offering his C/RTP analysis at trial.

First, ParkerVision failed to respond completely, or even reasonably, in response to Interrogatory No. 2 before the close of fact discovery as it was required to do. Fed. R. Civ. P. 26(e)(1)(A), 33(b)(3). As explained above, Dr. Steer's rebuttal report identifies a new C/RTP theory based on newly identified documents that ParkerVision could have and should have identified in response to Intel's Interrogatory No. 2. *See supra* at 5-6. Moreover, this late disclosure came even though Intel questioned ParkerVision's 30(b)(6) witness on this topic but he

[4] Ex. 14, Steer Rebuttal Rpt., Ex. D-1 ('902 patent chart) at 6 ("I have reproduced a block diagram of the circuit board with the Eddie-1 IC (shown in the figure below)" and showing block diagram), 10 (block diagram), 15-18, 20 (block diagram); Ex. 15, Steer Rebuttal Rpt., Ex. D-3 ('725 patent chart) at 6, 10, 14-15 (same); Ex. 16, Steer Rebuttal Rpt., Ex. D-6 ('673 patent chart) at 6, 10, 13, 16-18, 26-28, 33-35, 36 (same).

was unable to explain the alleged August 21, 1997 invention date or explain how any document supported it. *See supra* at 4.

As this Court recently explained, where—as here—"a party fails to disclose relevant information during fact discovery, Rule 37(c)(1) authorizes the exclusion of evidence that was not timely disclosed from use 'to supply evidence on a motion, at a hearing, or at a trial.'" *Ravgen, Inc. v. Lab. Corp. of Am. Holdings*, No. 6:20-cv-969-ADA, slip op. 4 (W.D. Tex. Oct. 4, 2022) (quoting Fed. R. Civ. P. 37(c)(1)). Indeed, the "***presumptive***" sanction is that the party "is not allowed to use that information" unless the party can show that the failure "was substantially justified or is harmless." *Id.*; *see also Flores v. AT&T Corp.*, 2019 WL 2746774, at *2 (W.D. Tex. Mar. 27, 2019) ("[T]he party facing sanctions under Rule 37(c) has the burden of demonstrating that a violation of Rule 26 was substantially justified or is harmless."). This rule specifically applies where, as here, a party fails to disclose theories and evidence in its interrogatory responses. *Elbit Sys. Land & C4I Ltd. v. Hughes Network Sys., LLC*, 2017 WL 2651618, at *10-12 (E.D. Tex. Jun. 20, 2017) (striking non-infringing alternatives offered for the first time in expert's rebuttal report because they were not disclosed in interrogatory response); *see Huawei Techs. Co. v. T-Mobile US, Inc.*, 2017 WL 4619791, at *2 (E.D. Tex. Oct. 16, 2017) ("[I]nterrogatory responses … narrow issues and set boundaries for trial.").[5]

[5] The fact that these late-disclosed documents were ***produced*** during fact discovery—alongside the nearly 300,000 other documents ParkerVision provided to Intel—is irrelevant. The relevant question is whether ParkerVision sufficiently disclosed its intent to rely on these materials to support its C/RTP arguments. *E.g.*, *Apple Inc. v. Samsung Elecs. Co.*, 2012 WL 2499929, at *1 (N.D. Cal. June 27, 2012) ("[M]any of the expert reports offer theories or rely on evidence never previously disclosed as required. Even if disclosed somewhere, the parties have forced each other to comb through the extraordinarily voluminous record to find them, rather than simply amending their contentions or interrogatory responses as they should. ***This is unacceptable***."). As explained above, ParkerVision did not do so here.

Second, ParkerVision cannot meet its burden of showing that its delay was substantially justified or harmless. To the contrary, ParkerVision has offered no justification for its delay, which causes significant and irreparable prejudice to Intel. For instance,

- ParkerVision's late disclosure precluded Intel from adequately testing the purported theory and facts—including investigating the more-than 1,000 newly identified documents—during fact discovery. Intel attempted to do so, but ParkerVision's 30(b)(6) witness on C/RTP could not provide any explanation or identify any document to support ParkerVision's claimed August 21, 1997 invention date. *See supra* at 4.
- Intel investigated prior art and prepared invalidity positions based, in part, on ParkerVision's interrogatory responses and the fact that ParkerVision had presented no theory or evidence to support a claimed August 21, 1997 invention date.
- ParkerVision's late disclosure likewise precluded Intel's expert from adequately addressing this theory and documents. Intel's expert Dr. Subramanian was unable to address ParkerVision's new theory and newly identified documents in either his opening or rebuttal expert report (because it came after he had served both of his expert reports), and he based his invalidity analysis, at least in part, on ParkerVision's failure to identify any basis for an August 21, 1997 invention date.

See Elbit, 2017 WL 2651618, at *10-12 (prejudice from failure to disclose non-infringing alternative theory and evidence during fact discovery "is significant" because plaintiff "has not had a chance to test the underlying merits of [defendants' expert's] conclusions through discovery"); *Finjan, Inc. v. Symantec Corp.*, 2018 WL 620169, at *2 (N.D. Cal. Jan. 30, 2018) ("If the theory is new, ***prejudice is inherent*** in the assertion of a new theory after discovery has closed." (citation and punctuation omitted)).

Because ParkerVision cannot show that its failure to timely disclose its C/RTP theory and underlying documents was substantially justified or harmless, ParkerVision cannot "use that information … to supply evidence on a motion, at a hearing, or at a trial." Fed. R. Civ. P. 37(c)(1).

ii. Dr. Steer's C/RTP opinions should be excluded under *Daubert* and FRE 702.

Dr. Steer's C/RTP opinions should be excluded under *Daubert* and FRE 702 for the additional reason that his methodology in evaluating ParkerVision's alleged reduction to practice was fundamentally unsound: he has failed to provide any evidence of an actual reduction to practice, has failed to apply the Court's claim construction for the "storage element" limitations, and has applied no methodology whatsoever to show that ParkerVision's alleged reduction to practice satisfied the "storage element" claim limitations.

To show conception, "a party must show possession of every feature recited in the [claim], and that every limitation of the [claim] must have been known to the inventor at the time of the alleged conception." *Coleman v. Dines*, 754 F.2d 353, 359 (Fed. Cir. 1985). Similarly, to constitute an actual reduction to practice, the alleged invention as reduced to practice must (1) meet exactly "every element" of the claim, and (2) "operate[] for its intended purpose." *Eaton v. Evans*, 204 F.3d 1094, 1097 (Fed. Cir. 2000). The patentee must also introduce "independent evidence" to "corroborate" the alleged reduction to practice. *Medichem, S.A. v. Rolabo, S.L.*, 437 F.3d 1157, 1169 (Fed. Cir. 2006). Dr. Steer's C/RTP analysis does not and cannot meet these requirements because of the fundamental flaws in his analytical approach.

Each claim at issue in this motion requires an "energy storage module" ('902 patent, claim 5), a "storage module" ('725 patent, claim 6), an "energy storage device" ('673 patent, claim 17),

or a capacitor that is part of an energy transfer system ('673 patent, claim 5).[6] The Court has construed such "storage element" terms to require a module or device "that stores non-negligible amounts of energy from an input electromagnetic signal." For these "storage element" limitations, Dr. Steer points to a capacitor on a circuit board that allegedly contained an Eddie-1 chip, citing a circuit board schematic allegedly dated August 21, 1997 (one of the documents that, as discussed above, ParkerVision failed to identify during fact discovery). *See, e.g.*, Ex. 14, Steer Rebuttal Rpt., Ex. D-1 at 5-6. Dr. Steer's analysis is facially unsound for two reasons.

First, as an initial matter, Dr. Steer fails to present ***any*** evidence that the August 21, 1997 circuit board schematic was ever actually implemented in an actual physical embodiment. That failure alone is sufficient to disqualify Dr. Steer's alleged conception and reduction to practice analysis. *See Cooper v. Goldfarb*, 154 F.3d 1321, 1327 (Fed. Cir. 1998) ("In order to establish an ***actual*** reduction to practice, the inventor must prove that: (1) he constructed an embodiment or

[6] Dr. Steer and ParkerVision have been clear that all the asserted claims require an energy transfer system and therefore a "storage" element. *See* Ex. 13, Steer Rebuttal Rpt., ¶2333 ("The asserted claims of the patents-in-suit recite various systems/apparatus for down-conversion an RF signal using a 'storage' element/module/ device and a low impedance load. The Court has construed the 'storage' terms to refer to an element/module/device of an energy transfer system. Energy transfer system is another name for energy sampling. Thus, ***a characteristic of all of the asserted claims is they incorporate the concept of using energy sampling to down-convert***."); *id.*, ¶544 (distinguishing prior art as allegedly not disclosing "an energy transfer system as set forth in the patents-in-suit."); Ex. 20, Steer Opening Rpt., ¶464 (defining "an energy transfer system" as "us[ing] … a 'storage' capacitor … for storing and discharging non-negligible amounts of energy."); *see also* Ex. 21, Subramanian Rebuttal Rpt., ¶¶578-607.

performed a process that met all the limitations of the interference count; and (2) he determined that the invention would work for its intended purpose.").[7]

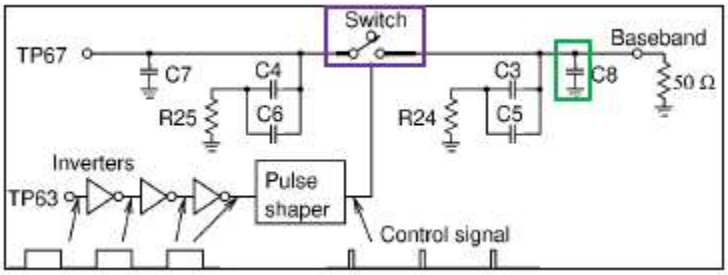
Second, Dr. Steer never applies the Court's claim construction for the "storage element" terms and therefore never shows that the alleged ParkerVision circuit board contained a storage element that stored "non-negligible amounts of energy." Indeed, Dr. Steer never makes ***even an assertion—much less the required showing with corroboration—***that any capacitor in the alleged ParkerVision circuit board stored the non-negligible amounts of energy required by the Court's claim construction. *See OneSubsea IP UK Ltd. v. FMC Techs., Inc.*, 2020 WL 7263266, at *5-*7 (S.D. Tex. 2020) (excluding expert's infringement opinion because expert did not "properly consider" an agreed claim construction and "misinterpret[ed]" other claim constructions; "Expert opinions that are inconsistent with the established constructions of claim terms are irrelevant and

[7] In addition to not presenting any evidence that the August 21, 1997 circuit board schematic was ever built, Dr. Steer's claim charts improperly cite a different alleged ParkerVision circuit board that Boeing allegedly tested in April 1998. *See, e.g.*, Ex. 14, Steer Rebuttal Rpt., Ex. D-1 ('902 patent chart) at 6-9 (showing circuit board schematic and simplified block diagram for circuit board allegedly used by Boeing). That circuit board's configuration and component values, however, are facially and significantly different from the alleged August 21, 1997 circuit board. Moreover, Dr. Steer never identifies any alleged storage element on the Boeing circuit board or makes any assertion or showing that any capacitor on that board stored non-negligible amounts of energy.

In addition, when attempting to establish that the alleged August 21, 1997 circuit board practiced the asserted claims, Dr. Steer improperly relies on evidence relating to the different Boeing circuit board. Specifically, he relies on the structure of the alleged August 21, 1997 circuit board but calculates a "percentage of energy discharged" based on the RF and local oscillator (LO) signals allegedly used in the Boeing circuit board testing—even though there is no evidence those frequencies were ever used with the alleged August 21, 1997 circuit board. Ex. 14, Steer Rebuttal Rpt., Ex. D-1 ('902 patent chart) at 16 (analyzing Dr. Steer's block diagram of the alleged April 21, 1997 circuit board schematic), 16 ("Using the frequencies [of the RF and LO signals] provided in the Boeing Report, I determined that the percentage of energy discharged from the capacitor [C8 in the April 21, 1997 schematic] (between sampling apertures) is 72.7%."); Ex. 15, Steer Rebuttal Rpt., Ex. D-3 ('725 patent chart) at 13-15 (same); Ex. 16, Steer Rebuttal Rpt., Ex. D-6 ('673 patent chart) at 16-18, 31-35 (same). Such mixing and matching of evidence regarding two different circuit boards cannot support a reduction to practice in either August 1997 or April 1998.

unhelpful to the factfinder."); *Mission Pharmacal Co. v. Virtus Pharm., LLC*, 2014 WL 12480016, at *4 (W.D. Tex. Sept. 12, 2014) (excluding expert testimony that was inconsistent with the Court's construction "because it is irrelevant, could confuse the jury, and would not 'help the trier of fact ... to determine a fact in issue'" (citing Fed. R. Evid. 702)).

Dr. Steer specifically identifies capacitor C8 (below in green) as the alleged storage element in the alleged ParkerVision circuit board (*see, e.g.*, Ex. 14, Steer Rebuttal Rpt., Ex. D-1 at 10, 13).



But Dr. Steer's analysis of the "storage element" limitations (an example of which is reproduced below from Dr. Steer's '902 patent chart) fails to state ***anything*** about whether that capacitor stores non-negligible amounts of energy.

> The single-ended capacitor (C8, green box (above)) functions as a module of an energy transfer system. An energy transfer system transfers non-negligible amounts of energy from an input electromagnetic signal to a low impedance load to form a down-converted signal. The input electromagnetic signal is related to the carrier signal and is not previously down-converted.
>
> In the Eddie-1 design, a down-converted signal is being created from (1) energy transferred from the switch module to a low impedance load and (2) energy discharged from the energy storage module to the low impedance load. The energy from the energy storage module fills in the gaps between discrete signal portions being output from the switch module.
>
> In particular, the recursive closing/opening of the switch module (transistors M12-M17) periodically couples the electromagnetic signal (shown along the red path above) to an energy storage module. During a sampling aperture of the energy transfer signal (LO1), for example, the switch module (transistors M12-M17) closes (the switch is "ON") and energy from the electromagnetic signal is directed to the energy storage module and to a low impedance load (50 Ω termination, shown in the brown box above). Between sampling apertures of the energy transfer signal, the switch module remains open (the switch is "OFF"), preventing energy from the electromagnetic signal from passing through the switch and discharging energy stored in the energy storage module to the low impedance load. The sampling, charging, and discharging process outputs a down-converted signal.

Ex. 14, Steer Rebuttal Rpt., Ex. D-1 at 13-14; *see also* Ex. 15, Steer Rebuttal Rpt., Ex. D-3 ('725 patent chart) at 10, 13-14; Ex. 16, Steer Rebuttal Rpt., Ex. D-6 ('673 patent chart) at 31-35; *id.* at 10, 13-18. Dr. Steer's statement that "[a]n energy transfer system transfers non-negligible amounts

of energy from an input electromagnetic signal to a low impedance load to form a down-converted signal," *id.*, describes his view of what an energy transfer system is—not the specific ParkerVision circuit board—and in any event it refers to the amount of energy transferred ***to the load***, not the amount of energy stored ***on the alleged storage element***. Moreover, when he describes the purported operation of the ParkerVision circuit board, Dr. Steer states only that the closing/opening of the switch "periodically couples" the signal "to an energy storage module." *Id.* That says nothing about the ***amount*** of energy stored on the capacitor. *See id.* Indeed, Dr. Steer himself affirmatively argues elsewhere that merely because a system transfers energy from a switch to a capacitor does not make it the claimed energy transfer system. *See, e.g.*, Ex. 20, Steer Opening Rpt., ¶575 ("Merely because energy is being transferred from a switch to a capacitor does not make a system an energy transfer system."); *id.*, ¶¶223-25 (distinguishing claimed invention from "voltage sampling" system in which "the switch closes and energy from the RF signal … is sent to the capacitor").[8]

Dr. Steer's infringement analysis highlights the fundamental flaws with his C/RTP opinions. Unlike in his C/RTP analysis, in his infringement analysis, he acknowledges the "non-negligible amounts of energy" requirement and spends many pages attempting (albeit unsuccessfully) to address that requirement. Indeed, he employs detailed circuit simulations and calculations to allegedly show the amount of energy stored on Intel capacitors—simulations and

[8] Dr. Steer's claim charts for the '725 and '673 patents include additional analysis directed to other claim requirements—such as a "percentage of energy discharged" calculation that, according to Dr. Steer, indicates that "the Eddie-1 is an energy transfer system." Ex. 15, Steer Rebuttal Rpt., Ex. D-3 ('725 patent chart) at 15; Ex. 16, Steer Rebuttal Rpt., Ex. D-6 ('673 patent chart) at 18, 35. That calculation, however, purports to show only what percentage of the energy stored on the capacitor is discharged; none of Dr. Steer's additional analysis asserts or shows that the "amount" of energy stored on the capacitor is "non-negligible." Moreover, as noted above in footnote 7, Dr. Steer's "percentage of energy discharged" calculation is based on an unsupported mixing and matching of different circuit boards and cannot support any claimed reduction to practice.

calculations he somehow failed to perform when attempting to show ParkerVision's alleged C/RTP. *See, e.g.*, Ex. 20, Steer Opening Rpt., ¶¶591, 637-38 (citing App. E, Fig. IV.B.7, 8, 9, 10, Fig. IV.C.7, 8, 9, 10, Fig. IV.D.7, 8, 9, 10, Fig. IV.E.7, 8, 9, 10, Fig. IV.F.7, 8, 9, 10); Ex. 25, Appendix J-1 at 21 [redacted] *See* Section XXVIII of the Expert Report; Figures IV.E in Appendix E.").

Dr. Steer's C/RTP opinions are also inconsistent with his validity analysis. Dr. Steer's rebuttal report attempts to distinguish multiple Intel prior art references on the grounds that they do not store enough energy to "meet cellular specifications/telecommunication standards." *See, e.g.*, Ex. 13, Steer Rebuttal Rpt., ¶593 ("[T]he Razavi capacitors must store non-negligible amount of energy (energy distinguishable from noise), which means that enough energy must be transferred into Razavi's capacitors (and Razavi's capacitors must store enough energy) to overcome noise in the system to be able to meet specifications (i.e., meet cellular specifications / telecommunication standards)."); *id.*, ¶598 ("Dr. Subramanian has not provided any evidence that the capacitors in Razavi's configuration store enough energy so that devices, into which the Razavi circuit is incorporated into, would work i.e., meet telecommunications standards."). But when analyzing ParkerVision's alleged C/RTP, Dr. Steer conveniently ignores this alleged requirement and makes no attempt to show that the ParkerVision circuit board met any telecommunication standard.

In short, Dr. Steer's C/RTP analysis fails to meet even minimal standards of reliability because it ignores the Court's "storge element" claim construction and relies on only the naked

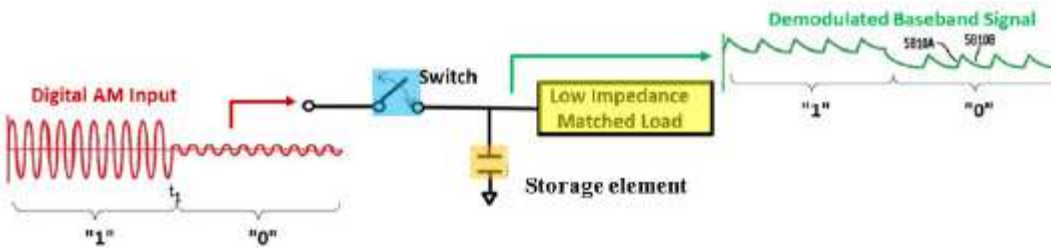
assertion that a storage element existed. Allowing Dr. Steer to present such an assertion that is unsupported by any methodology and that is inconsistent with the requirements of the Court's claim construction would only confuse the jury. Dr. Steer's C/RTP analysis for the claims identified in this motion is not reliable and should be excluded. *See Gen. Elec. Co. v. Joiner*, 522 U.S. 136, 146 (1997) ("[N]othing in either *Daubert* or the Federal Rules of Evidence requires a district court to admit opinion evidence that is connected to existing data only by the *ipse dixit* of the expert. A court may conclude that there is simply too great an analytical gap between the data and the opinion proffered."); *Cooper*, 154 F.3d at 1328 ("[T]he physical embodiment relied upon as an actual reduction to practice must include every limitation of the count. … What this means is that … Cooper was required to establish that Dr. Sharp's graft had fibril lengths within the parameters of the count. We agree with the Board that Cooper failed to make the requisite showing.").

B. Dr. Steer's Infringement Opinions Based On His Circuit-Level Simulations Should Be Excluded Under *Daubert* And FRE 702.

Federal Rule of Evidence 702 allows a qualified expert witness to testify if, among other things, (1) "the testimony is the product of reliable principles and methods," and (2) "the expert ***has reliably applied*** the principles and methods to the facts of the case." Dr. Steer's infringement analysis based on his circuit simulations fails that standard and should be excluded because he did not reliably apply standard circuit-simulation methodology. Specifically, his circuit-level simulations are based on indisputably inaccurate assumptions about Intel's products and therefore cannot produce reliable results as required under *Daubert* and FRE 702.

At a high-level of generality, the asserted claims require a down-conversion system in which a switch opens and closes a circuit, allowing energy from an electromagnetic signal to flow to a storage element that stores non-negligible amounts of energy and then discharges energy

forming the down-converted signal when the switch is off. Dr. Steer, for example, prepared the following figure to explain his view of ParkerVision's alleged "energy transfer (energy sampling) system":

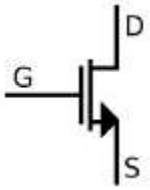


Ex. 20, Steer Opening Rpt., ¶233.

To analyze infringement, Dr. Steer prepared various circuit-level simulations that purported to model the overall operation of circuit configurations in the Intel products. *See, e.g.*, Ex. 20, Steer Opening Rpt., ¶¶568-571, 624-626; Ex. 22, Steer Opening Rpt., Appendix C ¶¶ 22, 48-52. To purportedly show that the Intel products use the claimed "energy transfer system," Dr. Steer used these simulations to, for example, generate various "waveforms" that allegedly showed relevant energy flows and signals in the Intel products. *See generally* Ex. 22, Steer Opening Rpt., Appendix C. Dr. Steer relied extensively on these simulation waveforms for his infringement conclusions. [redacted] *See, e.g.*, Ex. 20, Steer Opening Rpt., ¶¶576-78; Ex. 26, Steer Opening Rpt., Appendix N-1 at 53 ("[redacted] *see generally* Ex. 21, Subramanian Rebuttal Rpt., ¶¶681, 700-14, 735, 859-61.

Dr. Steer's simulation results are methodologically unreliable, however, because Dr. Steer simulated the Intel products using an ***idealized*** switch—i.e., a switch that does not exist in the real world—and [redacted]. Indeed, Dr. Steer's methodology is inexplicable because he used the ideal switch even though he had available to him—***and had used in other, separate simulations***—a real-world transistor model. *See* Ex. 21, Subramanian Rebuttal Rpt., ¶704; Ex. 20, Steer Opening Rpt., ¶¶568-71; Ex. 22, Steer Opening Rpt., Appendix C ¶¶48-52. As explained below, Dr. Steer's use of an ideal switch had major consequences for Dr. Steer's conclusions, which do not survive when a more realistic transistor model is used in Dr. Steer's own simulations.

In the Intel products, [redacted] There is no dispute that a FET is a specific circuit component with three terminals—a gate, source, and a drain (as shown below).



Dr. Steer states that, "[o]ne of the characteristics of a FET is that a controlling voltage at one terminal controls a current between two of the other terminals," and he states that FETs "can be used as a switch, but they could also be used in other ways such as to provide amplification or to provide a time-varying resistance." Ex. 20, Steer Opening Rpt., ¶¶84-85. When performing his circuit-level simulations for the Intel products, however, Dr. Steer did not use [redacted]. Instead, he modeled the Intel circuit configurations using idealized switches in place of the Intel transistors. *See* Ex. 20, Steer Opening Rpt., ¶¶622-626; Ex. 22, Steer Opening Rpt., Appendix C ¶¶21-24. Thus, instead of modeling the specific behavior of the Intel

transistors, Dr. Steer modeled the Intel transistors as devices that simply turn on and off immediately, with no transition between on and off states and with no other electrical characteristics. *See generally* Ex. 21, Subramanian Rebuttal Rpt., ¶¶681, 700-14, 735, 859-61.

As Dr. Subramanian explained in his Rebuttal Report, "There are several significant and substantive differences between products that operate with an ideal switch compared to those that operate with a transistor." *Id.*, ¶702. Dr. Subramanian explained that transistor electrical effects such as "parasitic coupling capacitance" and "charge injection" are not captured by an ideal switch, and that the omission of these effects in Dr. Steer's circuit-level simulations has "significant effects on the waveforms generated by the simulated circuitry." *Id.*

Indeed, when Dr. Subramanian ran Dr. Steer's own simulations but [redacted]. *See id.*, ¶704; Ex. 20, Steer Opening Rpt. ¶¶568-71; Ex. 22, Steer Opening Rpt., Appendix C ¶¶48-52. [redacted] *See* Ex. 21, Subramanian Rebuttal Rpt., ¶708 ("[redacted]

[9] To be clear, [redacted] *See* Subramanian Rebuttal Rpt., ¶¶608-694, 747-768, 794-811, 817-831.

[redacted] *see also id.*, ¶¶851-61.[10]

[redacted] By ignoring all of that additional electrical behavior, Dr. Steer's circuit-level simulations did not "reliably appl[y]" standard circuit-simulation methodology (FRE 702) and made his infringement analysis fundamentally unreliable. It is undisputed that every circuit simulation involves some level of simplification. But Dr. Steer's simplification of the Intel products for his circuit-level simulations here was methodologically inconsistent ***with his own separate simulations*** where he used a real-world transistor model—a model that he indisputably could have used—but chose not to—in order to model Intel's products in his circuit-level simulations.

IV. CONCLUSION

For the foregoing reasons, Intel respectfully requests that the Court exclude the opinions of Dr. Steer related to (1) the alleged conception, reduction to practice, and diligence for claim 5

[10] At his deposition, Dr. Steer criticized Dr. Subramanian's corrected version of Dr. Steer's simulations, asserting that Dr. Subramanian had inaccurately modeled the [redacted] *See* Ex. 23, Steer Dep. at 399:25-400:22. But as Dr. Subramanian explained at his deposition, even if Dr. Steer were right that the [redacted] should have been modeled differently, this detail of the simulation would have no effect on the relevant results of the simulations (*see* Ex. 24, Subramanian Dep. at 675:6-676:20), and Dr. Steer has never asserted or offered any evidence that the simulation results would have changed in a relevant manner if the [redacted] had been modeled differently.

of the ’902 patent, claim 6 of the ’725 patent, and claims 5 and 17 of the ’673 patent; and (2) alleged infringement based on purported circuit-level simulations of the Intel products-at-issue.

Dated: October 28, 2022

Respectfully submitted,

/s/ J. Stephen Ravel

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CERTIFICATE OF SERVICE

I hereby certify that all counsel of record who are deemed to have consented to electronic service are being served with a copy of the foregoing document via electronic mail on October 28, 2022.

/s/ J. Stephen Ravel
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