

IN THE UNITED STATES DISTRICT COURT  
FOR THE WESTERN DISTRICT OF TEXAS  
WACO DIVISION

PARKERVISION, INC.,  
*Plaintiff*

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W-20-CV-00562-ADA

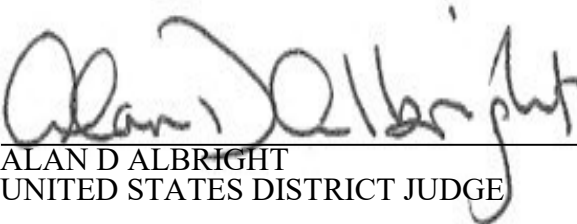
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INTEL CORPORATION,  
*Defendant*

**AMENDED CLAIM CONSTRUCTION ORDER**

The Court previously entered a Claim Construction order in this case on July 22, 2021.  
The Court now amends that order to correct an error in its final construction for “storage module.”

**SIGNED** this 22nd day of October, 2021.

  
ALAN D ALBRIGHT  
UNITED STATES DISTRICT JUDGE

Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Final Construction
<p>“under-sample” / “undersamples” / “under-sampling”</p> <p>'706 patent, claims 1, 6, 7, 28, 34</p>	<p>“sampling at an aliasing rate” or “sampling at less than or equal to twice the frequency of the input signal”</p>	<p>“sample[s/ing] at less than or equal to twice the frequency of the input signal using negligible apertures (i.e., pulse widths) that tend towards zero time in duration”</p>	<p>“sampling at an aliasing rate” or “sampling at less than or equal to twice the frequency of the input signal”</p>
<p>“storage module”</p> <p>'706 patent, claims 105, 114, 164, 175, 179, 186, 190</p>	<p>“a module of an energy transfer system that stores non-negligible amounts of energy from an input electromagnetic signal for driving a low impedance load”</p>	<p>“a module that stores a non-negligible amount of energy from an input electromagnetic (EM) signal”</p>	<p>“a module of an energy transfer system that stores non-negligible amounts of energy from an input electromagnetic signal for driving a low impedance load”</p>
<p>“switch”</p> <p>'706 patent, claims 105, 164, 175, 186; '108 patent, claim 1</p>	<p>“an electronic device for opening and closing a circuit as dictated by an independent control input”</p>	<p>“an electronic device for opening and closing a circuit”</p>	<p>Plain-and-ordinary meaning wherein the plain-and-ordinary meaning is “an electronic device for opening and closing a circuit as dictated by an independent control input”</p>

Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Final Construction
<p>“a down-convert and delay module to under-sample an input signal to produce an input sample of a down-converted image of said input signal, and to delay said input sample”</p> <p>'706 patent, claims 1, 7</p>	<p>Plain and ordinary meaning</p>	<p><b>Function:</b> under-sample an input signal according to a control signal to produce an input sample of a down-converted image of said input signal, and to delay said input sample</p> <p><b>Structure:</b> the down convert and delay module 2624 in Fig. 26 and described at 26:1-27:21 and 28:2041, that includes the switches 2650 and 2654, and the capacitors 2652 and 2656; and equivalents thereof</p>	<p>Not subject to § 112, ¶ 6. Plain-and-ordinary meaning.</p>
<p>“a frequency translator to produce a sample of a down-converted image of an input signal, and to delay said sample”</p> <p>'706 patent, claim 34</p>	<p>Plain and ordinary meaning</p>	<p><b>Function:</b> produce a sample of a down-converted image of an input signal according to a control signal, and to delay said sample</p> <p><b>Structure:</b> the down convert and delay module 2624 in Fig. 26 and described at 26:1-27:21 and 28:2041, that includes the switches 2650 and 2654, and the capacitors 2652 and 2656; and equivalents thereof.</p>	<p>Not subject to § 112, ¶ 6. Plain-and-ordinary meaning.</p>

Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Final Construction
<p>“said input sample”, “said sample”</p> <p>'706 patent, claims 1, 6, 7, 34</p>	<p>Plain and ordinary meaning</p>	<p>“the sample of the image that has been down-converted”</p>	<p>Plain-and-ordinary meaning</p>
<p>“delay module to delay instances of an output signal”, “delay modules to further delay one or more of said delayed and down-converted input samples”</p> <p>'706 patent, claims 1, 7, 34, 140</p>	<p>Plain and ordinary meaning</p>	<p><b>Function:</b> delay instances of an output signal / further delay one or more of said delayed and downconverted input samples</p> <p><b>Structure:</b> structure including “first delay module 2628,” “second delay module 2630” shown in Fig 26, “delay module 3204” shown in Fig. 32 and described at 35:1-18; the sample and hold circuit 4501 and 4503 in Fig. 45 and described at 32:44-33:19; or an analog delay line having a combination of capacitors, inductors and/or resistors described at 35:19-27; or equivalents thereof.</p>	<p>Not subject to § 112, ¶ 6. Plain-and-ordinary meaning.</p>

Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Final Construction
<p>“harmonic”, “harmonics”</p> <p>'706 patent, claims 1, 6, 7, 28, 34; '508 patent, claim 1</p>	<p><b>Harmonic:</b> “A sinusoidal component of a periodic wave that has a frequency that is an integer multiple of the fundamental frequency of the periodic waveform and including the fundamental frequency as the first harmonic”</p> <p><b>Harmonics:</b> “A frequency or tone that, when compared to its fundamental or reference frequency or tone, is an integer multiple of it and including the fundamental frequency as the first harmonic”</p>	<p><b>Harmonic:</b> “A sinusoidal component of a periodic wave that has a frequency that is an integer multiple of the fundamental frequency of the periodic wave”</p> <p><b>Harmonics:</b> “Sinusoidal components of a periodic wave each of which have a frequency that is an integer multiple of the fundamental frequency of the periodic wave”</p>	<p>Plain-and-ordinary meanings:</p> <ul style="list-style-type: none"> <li>• <b>Harmonic:</b> “A sinusoidal component of a periodic wave that has a frequency that is an integer multiple of the fundamental frequency of the periodic waveform and including the fundamental frequency as the first harmonic”</li> <li>• <b>Harmonics:</b> “A frequency or tone that, when compared to its fundamental or reference frequency or tone, is an integer multiple of it and including the fundamental frequency as the first harmonic”</li> </ul>
<p>“pulse widths that are established to improve energy transfer”</p> <p>'706 patent, claim 2</p>	<p>Plain and ordinary meaning, or Pulse widths that use non-negligible apertures for energy transfer</p>	<p>Indefinite</p>	<p>Not indefinite. Plain-and-ordinary meaning.</p>

Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Final Construction
<p>“means for under-sampling an input signal to produce an input sample of a down-converted image of said input signal”</p> <p>'706 patent, claim 6</p>	<p><b>Function:</b> under-sampling an input signal to produce an input sample of a down-converted image of the input signal and under-sampling the input signal according to a control signal</p> <p><b>Structure:</b> switch 2650 in Fig. 26; switch 5308 in Figs. 53A/53A-1; and equivalents thereof</p>	<p><b>Function:</b> under-sampling an input signal to produce an input sample of a down-converted image of said input signal and under-sampling the input signal according to a control signal</p> <p><b>Structure:</b> the switch 2650 and the capacitor 2652 in Fig. 26 and described at 26:1-27:21, 28:20-28, and 39:25-28; the switch 5308 and capacitor 5310 in Fig. 53A and described at 28:46-47; the switch 5308 and capacitor 5310 in Fig. 53A-1 and described at 28:52-56 and equivalents thereof.</p>	<p>Subject to § 112, ¶ 6.</p> <p><b>Function:</b> under-sampling an input signal to produce an input sample of a down-converted image of said input signal and under-sampling the input signal according to a control signal</p> <p><b>Structure:</b> the switch 2650 and the capacitor 2652 in Fig. 26 the switch 5308 and capacitor 5310 in Figs. 53A/53A-1, and equivalents thereof.</p>
<p>“first delaying means for delaying said input sample”</p> <p>'706 patent, claim 6</p>	<p><b>Function:</b> delaying the input sample of a down-converted image of said input signal</p> <p><b>Structure:</b> capacitor 2656 in Fig. 26 or capacitor 5310 in Figs. 53A/53A1; and equivalents thereof</p>	<p><b>Function:</b> delaying said input sample</p> <p><b>Structure:</b> the switch 2654 and capacitor 2656 shown in Fig. 26 and described at 25:57-27:21 and 28:2028; and equivalents thereof.</p>	<p>Subject to § 112, ¶ 6.</p> <p><b>Function:</b> delaying said input sample</p> <p><b>Structure:</b> switch 2654 and capacitor 2656 shown in Fig. 26.</p>

Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Final Construction
<p>“second delaying means for delaying instances of an output signal”</p> <p>'706 patent, claim 6</p>	<p><b>Function:</b> delaying instances of an output signal</p> <p><b>Structure:</b> delay modules 1722A, 1722B, 1722C, etc. in FIG. 17; delay modules 1912, 1914 in Fig. 19; delay modules 2316, 2318 in Fig. 23; first delay module 2628, second delay module 2630 in Fig. 26; delay module 3204 shown in Fig. 32; sample and hold circuits 4501, 4503 shown in Fig. 45; analog delay line 3404 shown in Fig. 34 having a combination of capacitors, inductors, and/or resistors; and equivalents thereof</p>	<p><b>Function:</b> delaying instances of an output signal</p> <p><b>Structure:</b> structure including “first delay module 2628,” “second delay module 2630” shown in Fig 26 and described at 32:27-55, “delay module 3204” shown in Fig. 32 and described at 35:1-18; the sample and hold circuits 4501 and 4503 in Fig. 45 and described at 32:44-64; or an analog delay line having a combination of capacitors, inductors and/or resistors described at 35:19-27; and equivalents thereof.</p>	<p>Subject to § 112, ¶ 6.</p> <p>Function: delaying instances of an output signal</p> <p>Structure: delay modules 1722A, 1722B, 1722C, etc. in FIG. 17; delay modules 1912, 1914 in Fig. 19; delay modules 2316, 2318 in Fig. 23; first delay module 2628, second delay module 2630 in Fig. 26; delay module 3204 shown in Fig. 32; sample and hold circuits 4501, 4503 shown in Fig. 45; analog delay line 3404 shown in Fig. 34 having a combination of capacitors, inductors, and/or resistors; and equivalents thereof</p>

<p>“integral filter/frequency translator to filter and downconvert an input signal”</p> <p>’706 patent, claim 28</p>	<p>“a circuit having a unified input filter and frequency translator”</p>	<p><b>Function:</b> to filter and downconvert an input signal and to undersample said input signal according to a control signal</p> <p><b>Structure:</b> the Unified Downconvert and Filter (UDF) Module 2622 that includes:</p> <ol style="list-style-type: none"> <li>(1) the frequency translator 1108 having the down convert and delay module 2624;</li> <li>(2) a first delay module, including the delay module 2628 shown in Fig. 26, the delay module 3204 shown in Fig. 32 and described at 35:1-18, the sample and hold circuit 4501 or 4503 shown in Fig. 45 and described at 32:44-64, or the analog delay line having a combination of capacitors, inductors and/or resistors described at 35:19-27;</li> <li>(3) a second delay module including the delay module 2630 shown in Fig. 26, the delay module 3204 shown in Fig. 32 and described at 35:1-18, the sample and hold circuit 4501 or 4503 shown in Fig. 45 and described at 32:44-64, or</li> </ol>	<p>Not subject to § 112, ¶ 6. Plain-and-ordinary meaning wherein the plain-and-ordinary meaning is “a circuit having a unified input filter and frequency translator.”</p>
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the analog delay line having a combination of capacitors, inductors and/or resistors described at 35:19-27; a first scaling module, including the first scaling module 2632 shown in Fig. 26, the resistor attenuator 3602 shown in Fig. 36 and described at 35:44-55, or the amplifier/attenuator 3704 implemented using operational amplifiers, transistors, or FETs shown in Fig. 37 and described at 35:60-67;

(5) a second scaling module, including the second scaling module 2634 shown in Fig. 26, the resistor attenuator 3602 shown in Fig. 36 and described at 35:44-55, or the amplifier/attenuator 3704 implemented using the operational amplifiers, transistors, or FETs shown in Fig. 37 and described at 35:60-67;

(6) a first adder including, the adder 2625 in Fig. 26, adder 1720 in Fig. 17, the adder 2522 in Fig. 25, the

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		summer 3902 in Fig. 39, or the summer 4102 in Fig. 41; and a second adder, including the adder 2626 in Fig. 26, adder 1720 in Fig. 17, the adder 2522 in Fig. 25, the summer 3902 in Fig. 39, and the summer 4102 in Fig. 41; and equivalents thereof.	
"modulated signal" '706 patent, claim 127	"an electromagnetic signal at a transmission frequency having at least one characteristic that has been modulated by a baseband signal"	"a signal with physical characteristics varied to represent the transmitted information"	"an electromagnetic signal at a transmission frequency having at least one characteristic that has been modulated by a baseband signal"

“filter tuning means for tuning one or more filter parameters”

'706 patent, claim 134

**Function:** tuning one or more filter parameters

**Structure:** scaling modules 1716A, 1716B, 1716C, 1724A, 1724B, 1724C in Fig. 17; control signal generator 1790 in Fig. 17; input scaling module 1909 in Fig. 19; scaling modules 1916, 1918 in Fig. 19; scaling modules 2312, 2320, 2322 in Fig. 23; scaling module 2632, 2634 in Fig. 26; scaling module 3502 including resistor attenuator 3504, 3602 in Figs. 35, 36; scaling module 3702 including amplifier/attenuator 3704 in Fig. 37; control signal generator 4202 in Fig. 42; and equivalents thereof

**Function:** tuning one or more filter parameters

**Structure:** scaling modules including the resistor attenuator 3602 (shown in Fig. 36 and described at 35:44-55) or the amplifier/attenuator 3704 implemented using operational amplifiers, transistors, or FETS (shown in Fig. 37 and described at 35:60-67), each of the resistor attenuator 3602 and the amplifier/attenuator 3704 having tunable resistors, capacitors, or inductors (as described at 42:33-36); and equivalents thereof; **OR** the control signal generator 4202 (shown in Fig. 42 and described at 36:44-62 and 42:27-32) implemented with a tunable oscillator 4204 and an aperture optimizing module 4210 using tunable components (such as tunable resistors, capacitors, inductors, etc.) (described at 36:63-37:5 and 42:2732) and equivalents thereof.

Subject to § 112, ¶ 6.

**Function:** tuning one or more filter parameters

**Structure:** scaling modules 1716A, 1716B, 1716C, 1724A, 1724B, 1724C in Fig. 17; input scaling module 1909 in Fig. 19; scaling modules 1916, 1918 in Fig. 19; scaling modules 2312, 2320, 2322 in Fig. 23; scaling module 2632, 2634 in Fig. 26; scaling module 3502 including resistor attenuator 3504, 3602 in Figs. 35, 36; scaling module 3702 including amplifier/attenuator 3704 in Fig. 37; and equivalents thereof.

Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Final Construction
<p>“pulse shaping means for shaping a string of pulses from a reference signal”</p> <p>'508 patent, claim 1</p>	<p><b>Function:</b> shaping a string of pulses from a reference signal</p> <p><b>Structure:</b> pulse shaper 3900 in Fig. 39A; pulse shaping circuit/pulse shaper 4000 in Fig. 40A; pulse shaping circuit 4100 in Fig. 41; harmonic enhancement module 4602 in Fig. 46; signal shaper 5010 in Fig. 50; harmonic enhancement module 5124 in Fig. 51B-C; pulse shaper 5310 in Fig. 53; pulse shaper 5438 in Fig. 54A; pulse shaper 5438 in Fig. 55; pulse shaper 5632 in Fig. 56; pulse shaping circuit 5722 in Fig. 57A-C, pulse shaper 6216 in Fig. 62; pulse shaper 7812 in Fig. 78; and equivalents thereof</p>	<p><b>Function:</b> shaping a string of pulses from a reference signal</p> <p><b>Structure:</b> the pulse shaping circuit 3900 shown in Fig. 39A and described at 48:8-39, the pulse shaping circuit 4000 shown in Fig. 40A and described at 48:40-49:5, and the pulse shaping circuit 4100 shown in Fig. 41 and described at 49:6-26, which incorporates circuit element 4104 shown in Fig. 43 and described at 49:6-26; and equivalents thereof.</p>	<p>Subject to § 112, ¶ 6.</p> <p><b>Function:</b> shaping a string of pulses from a reference signal</p> <p><b>Structure:</b> the pulse shaping circuit 3900 shown in Fig. 39A and described at 48:8-39, the pulse shaping circuit 4000 shown in Fig. 40A and described at 48:40-49:5, and the pulse shaping circuit 4100 shown in Fig. 41 and described at 49:6-26, which incorporates circuit element 4104 shown in Fig. 43 and described at 49:6-26; and equivalents thereof.</p>

Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Final Construction
<p>“aperture generation means ... for generating a string of multiple pulses from said string of pulses”</p> <p>'508 patent, claim 1</p>	<p><b>Function:</b> generating a string of multiple pulses from said string of pulses</p> <p><b>Structure:</b> aperture generation module 7806 in Fig. 78 having gate(s) and delay(s) such as the aperture generation module shown in Fig. 79; and equivalents thereof</p>	<p><b>Function:</b> generating a string of multiple pulses from said string of pulses</p> <p><b>Structure:</b> the aperture generation module 7806 shown in Fig. 79 and described at 49:54-50:5; and equivalents thereof.</p>	<p>Subject to § 112, ¶ 6.</p> <p>Function: generating a string of multiple pulses from said string of pulses</p> <p>Structure: the aperture generation module 7806 shown in Fig. 79; and equivalents thereof.</p>
<p>“generating a string of multiple pulses from said string of pulses”</p> <p>'508 patent, claim 1</p>	<p>Plain and ordinary meaning</p>	<p>“generating a signal with multiple the number of pulses as said string of pulses”</p>	<p>Plain and ordinary meaning</p>

Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Final Construction
<p>“gating means for gating a bias signal under the control of said string of multiple pulses to generate a periodic signal having a plurality of harmonics at least one of which is at a desired frequency”</p> <p>'508 patent, claim 1</p>	<p><b>Function:</b> gating a bias signal under the control of said string of multiple pulses to generate a periodic signal having a plurality of harmonics at least one of which is at a desired frequency</p> <p><b>Structure:</b> the switches shown in Fig. 28A, 29A, 30A, 31A, 32A, 33A, 53, 54A, 55, 56, 57A-C; and equivalents thereof</p>	<p><b>Function:</b> gating a bias signal under the control of said string of multiple pulses to generate a periodic signal having a plurality of harmonics at least one of which is at a desired frequency</p> <p><b>Structure:</b> switch 2816 shown in Fig. 28A and described at 35:1436:24 and 45:47-46:37; GaAsFET 2901 shown in Fig. 29A and described at 36:25-50; GaAsFETs 3002 and 3004 shown in Fig. 30A and described at 36:25-50; switch 5312 shown in Fig. 53 and described at 58:63-59:13, switch 5636 shown in Fig. 56 and described at 60:66-61:10; switch 5420 shown in Fig. 54A and described at 60:1-22; switch 5724 shown in Figs. 57A-B and described at 65:49-55; and equivalents thereof.</p>	<p>Subject to § 112, ¶ 6.</p> <p><b>Function:</b> gating a bias signal under the control of said string of multiple pulses to generate a periodic signal having a plurality of harmonics at least one of which is at a desired frequency</p> <p><b>Structure:</b> the switches shown in Figs. 28A, 31A, 53, 54A, 55, 56, 57A-C; the GaAsFETs shown in 29A, 30A, 32A, and 33A, and equivalents thereof.</p>

Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Final Construction
"gating" '508 patent, claim 1	"changing between the open and closed states of a switch, as dictated by an independent control input"	"opening and closing a device to selectively output a signal"	Plain-and-ordinary meaning wherein the plain-and-ordinary meaning is "preventing or allowing the input signal to pass through the device based on an independent control signal"
"bias signal" '508 patent, claim 1; '108 patent, claim 1	"1) a signal having a steady, predetermined level; or 2) the modulating baseband signal"	"a signal having a fixed voltage or fixed current"	"a signal having a fixed voltage or fixed current"
"control signal" '108 patent, claim 1	Plain and ordinary meaning	"an oscillating signal that controls the first switch with a frequency that is a sub-harmonic of and lower than the desired output frequency"	Plain and ordinary meaning
"third switch" '108 patent, claim 1	Plain and ordinary meaning, or "switch" as construed by the Court in Case No. 6:20-cv-108	"a switch controlling whether the antenna transmits said signal"	"Switch": Plain-and-ordinary meaning wherein the plain-and-ordinary meaning is "an electronic device for opening and closing a circuit as dictated by an independent control input"
"pulse shaper" '108 patent, claims 6, 8	"circuitry that shapes an oscillating signal to generate a string of pulses"	"a circuit configured to enhance a desired harmonic by shaping an oscillating signal"	"circuitry that shapes an oscillating signal to generate a string of pulses"

