IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

PARKERVISION, INC., Plaintiff, vs. INTEL CORPORATION, Defendant.	Civil Action No. 6:20-cv-00562-ADA **JURY TRIAL DEMANDED**

INTEL CORPORATION'S REPLY CLAIM CONSTRUCTION BRIEF

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I. INTRODUCTION

Intel's responsive brief explained how its proposed claim constructions are supported by the intrinsic record—the claim language, the specification's explanation of the claimed technology, and the patent's description of the "present invention[s]" and how they purportedly differ from the prior art.

PV cannot reconcile its claim construction positions with this intrinsic evidence. For example, PV insists that a "bias signal" can be a "reference signal" that varies even though the '508 patent describes "bias signals" as "unvarying" and specifically distinguishes "bias signals" from "reference signals." *See infra* pp. 36-39. PV also cannot reconcile its positions with settled claim construction precedent. PV cites only a single case in its entire 45-page brief, and PV misstates the law in its effort to support its positions. In the context of § 112, ¶ 6, for instance, PV asserts that if a claim term is described in the patent as "us[ing] ***any*** structure," then the term "connotes structure and § 112, ¶ 6 does not apply." Br. 13 n.9.[1] That is directly contrary to settled Federal Circuit precedent. *Egenera, Inc. v. Cisco Sys., Inc.*, 972 F.3d 1367, 1374 (Fed. Cir. 2020) ("[t]he question is not whether a claim term recites ***any*** structure but whether it recites ***sufficient*** structure" to perform the claimed function (emphases in original)).

With neither the facts nor the law on its side, PV unfortunately resorts to invective and mudslinging. PV's brief is replete with unfounded allegations of "gamesmanship," "false narratives," "ruses," "tricks," "misrepresentations" and "half-truths." But PV's invective cannot substitute for reasoned analysis. PV's constructions should be rejected, and the claims should be construed consistent with the intrinsic evidence, as Intel has proposed.

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[1]As cited herein, "Br." refers to PV's reply brief (Dkt. 43), "Intel Br." refers to Intel's responsive brief (Dkt. 41), "PV Op. Br." refers to PV's opening brief (Dkt. 37), and "VDW Supp." refers to the supplemental declaration of Dr. Daniel van der Weide, filed herewith. All emphases and annotations are added, unless otherwise noted.

II. THE '706 PATENT

A. Down Convert and Delay Terms

Claim Term	Proposed Constructions
"a down-convert and delay module to under-sample an input signal to produce an input sample of a down-converted image of said input signal, and to delay said input sample"	**Intel:** **Function:** under-sample an input signal according to a control signal to produce an input sample of a down-converted image of said input signal, and to delay said input sample **Structure:** the down convert and delay module 2624 in Fig. 26 and described at 26:1-27:21 and 28:20-41, that includes the switches 2650 and 2654, and the capacitors 2652 and 2656; and equivalents thereof **PV:** Plain and ordinary meaning
"a frequency translator to produce a sample of a down-converted image of an input signal, and to delay said sample"	**Intel:** **Function:** produce a sample of a down-converted image of an input signal according to a control signal, and to delay said sample **Structure:** the down convert and delay module 2624 in Fig. 26 and described at 26:1-27:21 and 28:20-41, that includes the switches 2650 and 2654, and the capacitors 2652 and 2656; and equivalents thereof. **PV:** Plain and ordinary meaning

The parties dispute (1) whether § 112, ¶ 6 applies to these down-convert and delay terms,[2] and (2) if so, the corresponding structure.[3]

Whether § 112, ¶ 6 Applies. In its responsive brief, Intel established that these terms must be construed as means-plus-function under *Williamson v. Citrix Online, LLC*, 792 F.3d 1339 (Fed. Cir. 2015), because the term "module" is a generic, nonce term that fails to connote structure, and the descriptor "down-convert and delay"—like the related term "frequency translator"—merely describes a function, not a sufficiently definite structure. Intel Br. 3-7.

PV argues in reply that neither term should be construed as means-plus-function because

[2] PV addresses the term "frequency translator" in a separate section of its reply, but makes the same arguments as for "down-convert and delay module." Br. 12. Because PV's arguments for both terms are the same, Intel addresses those arguments in a single section.

[3] PV noted in its opening brief that the claimed function includes "under-sampl[ing] said input signal according to a control signal." PV Op. Br. 9 n.4. Intel responded with no objection to including that function in the proposed construction, and clarified through correspondence before PV filed its reply brief that it would add that function to its proposals.

"the '706 patent relates to circuits, which have *physical* components," and "[s]o long as the term connotes *any* structure, § 112, ¶ 6 does *not* apply." Br. 8-9 (emphases in original). The Federal Circuit has expressly rejected that argument. When deciding whether a term should be construed as means-plus-function, "[t]he question is ***not*** whether a claim term recites ***any*** structure but whether it recites ***sufficient*** structure" to perform the claimed function. *Egenera*, 972 F.3d at 1374 (first emphasis added).

PV criticizes Intel for allegedly "reimagining the law regarding §112, ¶ 6" (Br. 8), but it is PV that fundamentally misperceives the law. PV ***fails to cite a single case*** in support of its argument that disclosure of "any" structure takes a term outside of § 112, ¶ 6. The lack of case law support is not surprising: under PV's view, no term in a patent directed to a physical device would ***ever*** fall within § 112, ¶ 6, so long as the patentee could point to ***some*** related physical structures in the specification. The Federal Circuit has expressly rejected PV's argument:

> The Board's analysis implies that so long as a claim term has corresponding structure in the specification, it is not a means-plus-function limitation. This is not consistent with our prior decisions. Indeed, this view would seem to leave § 112, ¶ 6 without any application: any means-plus-function limitation that met the statutory requirements, i.e., which includes having corresponding structure in the specification, would end up not being a means-plus-function limitation at all.

MTD Prods. Inc. v. Iancu, 933 F.3d 1336, 1344 (Fed. Cir. 2019).

PV compounds its legal error by arguing that whether the "down-convert and delay terms" connote a "*specific*, *complete*, or *well-known* structure is irrelevant." Br. 9 (emphases in original). To the contrary, the Federal Circuit has repeatedly found that "a critical question" in determining whether to construe a term as means-plus-function "is whether 'the claim term is ***used in common parlance*** [i.e., ***well-known***] or by persons of skill in the pertinent art to designate structure,' including either a ***particular*** [i.e., ***specific***] ***structure*** or a class of structures"—not merely "any" structure, as PV argues (without supporting legal citation). *MTD Prods.*, 933 F.3d at 1341

(collecting cases).

PV next argues Dr. van der Weide's statement that "down-convert and delay module" does "not have well-understood structural meaning[]" is contradicted by Dr. Subramanian's declaration from the '474 IPR, where PV says Dr. Subramanian "was able to identify a 'down-conversion module' (switch and capacitor) in a 1998 prior art reference …." Br. 9. But the term "down-convert ***and delay*** module" differs from "down-conversion module" in a critical way—it ***delays*** the incoming sample. Nothing in Dr. Subramanian's IPR declaration contradicts Dr. van der Weide's explanation that the term at issue here ("down-convert and delay module") did not have a well understood meaning. Indeed, as Intel explained in its responsive brief, the '706 patent's alleged novelty is to combine down-conversion ***and*** filtering into an integrated "down-convert and delay module." Intel Br. 2-3. It therefore should not be surprising that in 1998, "down-convert and delay module" did not have a definite structure known to skilled artisans. Dkt. 41-9 [VDW] ¶¶56-58.

Finally, PV badly misstates the holding of *TEK Global v. Sealant Systems International, Inc.*, 920 F.3d 777 (Fed. Cir. 2019). *TEK Global* reached a narrow conclusion based on the specific evidence in that case. *Id.* at 787 ("We thus conclude that the intrinsic and extrinsic evidence in this case establishes that the term 'conduit' recites sufficiently definite structure to avoid classification as a nonce term and agree with the district court that SSI did not meet its burden to overcome the presumption against applying § 112, ¶ 6."). Nothing in *TEK Global* establishes a rule that structure recited in a dependent claim can transform a functional term in an independent claim (like "down-convert and delay module") into a structural, non-mean-plus-function term. Such a rule would allow a patentee to engage in functional claiming in an independent claim and yet avoid the means-plus-function consequences simply by reciting some structure in a dependent claim. The Federal Circuit has rejected such attempts to evade the rules of means-plus-function construction.

Mollhagen v. Witte, 18 F. App'x 846, 849 (Fed. Cir. 2001) (nonprecedential) ("[T]he stringencies of a means-plus-function limitation cannot be avoided by merely adding a dependent claim that recites the corresponding structure disclosed in the specification."); *see also Nomos Corp. v. Brainlab USA, Inc.*, 357 F.3d 1364, 1368-69 (Fed. Cir. 2004).

The corresponding structure. As explained in Intel's opening brief, the only structures the specification clearly links to the claimed function are the "Downconvert and Delay Module 2624" and the "Frequency Translator 1108" in Figure 26—which each include ***two*** switch-capacitor pairs (one to down-convert the incoming signal, and the second to delay it). Intel Br. 5. PV does not dispute the claimed function or that clear linkage, but argues the structure should also include (1) the black boxes 1708, 1908, and 2308 in Figures 17, 19, 23 and (2) the ***single*** switch-capacitor pairs illustrated in Figures 53A, and 53A-1. Br. 10-11. PV is wrong on both counts.

First, the reason that black boxes 1708, 1908, and 2308 do not belong in the construction is not, as PV asserts, because the structure for this term is "spread out amongst multiple, related figures." Br. 11. Intel's constructions include many components where the structure is disclosed across multiple figures. Instead, black boxes 1708, 1908, and 2308 do not belong in the construction because they are empty boxes: Figures 17, 19, and 23 identify the "Downconvert and Delay Module(s)" 1708, 1908, and 2308 as functional blocks, without any disclosure of structure—i.e., specific circuitry. The Federal Circuit has made clear that the patentee must clearly link specific structure, not merely black boxes, with a means-plus-function term. *Biomedino, LLC v. Waters Techs. Corp.*, 490 F.3d 946, 948-53 (Fed. Cir. 2007) ("control means for automatically operating [a] valve[]" indefinite where specification disclosed only a "black box" and a general statement that known structure could be used); *ePlus, Inc. v. Lawson Software, Inc.*, 700 F.3d 509, 518 (Fed. Cir. 2012) (term indefinite where patentee relied on "black box" for structure; "step 114

in Figure 3, to which [patentee] refers …, is just a black box that represents the purchase-order-generation ***function*** without any mention of a corresponding structure." (emphasis in original)).

Notably, PV is not proposing to include black boxes 1708, 1908, and 2308 ***as implemented with the actual circuitry that the patent discloses for the "down-convert and delay" function***. Rather, PV is proposing to include these black boxes ***as black boxes***, thus attempting to expand this term to include any circuitry. As the Federal Circuit has held, that is precisely what §112, ¶ 6 prohibits: "It is not enough that a means-plus-function claim term correspond to every known way of achieving the claimed function; instead, the term must correspond to 'adequate' structure in the specification that a person of ordinary skill in the art would be able to recognize and associate with the function in the claim." *Synchronoss Techs., Inc. v. Dropbox, Inc.*, 987 F.3d 1358, 1367 (Fed. Cir. 2021) (term "user identifier module" was means-plus-function limitation and indefinite because specification failed to disclose structure sufficient to achieve function of identifying a user); *see also Med. Instrumentation & Diagnostics Corp. v. Elekta AB*, 344 F.3d 1205, 1211 (Fed. Cir. 2003) ("If the specification is not clear as to the structure that the patentee intends to correspond to the claimed function, then the patentee has not paid that price. … Such is impermissible under the statute.").[4]

Second, PV is wrong that Figures 53A and 53A-1 (each of which discloses only a single switch-capacitor pair) should be included as sufficient structure for these terms. Br. 11. The claims require "a down-convert and delay module" and thus are clearly linked to the "Downconvert and

[4] PV also argues that black boxes 1708, 1908, and 2308 constitute structure because they "have physical inputs/outputs connected to certain other components." Br. 11. But these inputs/outputs merely connect the black boxes to other structures; they do not perform the required down-convert and delay function and therefore are not corresponding structure. *See Asyst Techs., Inc. v. Empak, Inc.*, 268 F.3d 1364, 1371 (Fed. Cir. 2001) ("The corresponding structure to a function set forth in a means-plus-function limitation must actually perform the recited function, not merely enable the pertinent structure to operate as intended ….").

Delay Module 2624" and the "Frequency Translator 1108" in Figure 26, each of which includes ***two*** switch-capacitor pairs (one to down-convert the incoming signal, and the second to delay it).[5] PV asserts that the aliasing modules in Figures 53A and 53A-1 could be the down-convert and delay module because "[t]he opening and closing of a switch down-converts an input signal to produce a sample and a *capacitor delays the sample*." Br. 11 (emphasis in original). But the specification describes the aliasing modules as performing ***only*** down-conversion, ***not*** as performing the required delay, and the specification never describes (much less clearly links) a single capacitor as performing the delay. *See, e.g.*, '706, 28:42-46 ("FIG. 53A illustrates an aliasing module 5300 … for down-conversion."); VDW Supp. ¶¶34-35.[6]

B. "said input sample", "said sample"

Proposed Constructions
Intel: "the sample of the image that has been down-converted"
PV: Plain and ordinary meaning

PV argues that Intel's proposal is a "ruse," that it somehow "negat[es] the claimed relationship between the sample and input signal," and that Intel allegedly "re-write[s]" the claim. Br. 12. PV's invective misses the mark. Intel applies the basic rules of antecedent basis. The antecedent basis for "***said*** input sample"/"***said*** sample" is "an input sample of a down-converted image of said input signal." Consistent with that, Intel has simply defined "said input sample"/"said sample" with the

[5] PV suggests Figures 53A and 53A-1 should be included as structure because down-convert and delay modules 1708, 1908, 2308 "are described in the specification as being the aliasing module 5300 … of Figures 53A or 53A-1." Br. 3. PV cites column 28, but that column actually says "the downconvert and delay module 2624" from ***Figure 26***—not Figures 53A or 53A-1—"represents an example implementation of the down-convert and delay modules described herein, such as 1708 in FIG. 17, 1908 in FIG. 19, and 2308 in FIG. 23, and 2514 in FIG. 25." '706, 28:20-23.

[6] If Figures 53A and 53A-1 were included ***solely*** as corresponding to the down-conversion function—and not as purported structure for the entire "down-convert ***and delay***" function—Intel would not object. But Figures 53A and 53A-1 are not clearly linked to both "down-convert ***and*** delay" and therefore are not sufficient structure for the claimed function.

simpler, substantively identical language: "the sample of the image that has been down-converted."

C. "delay module to delay instances of an output signal", "delay modules to further delay one or more of said delayed and down-converted input samples"

Proposed Constructions
Intel: **Function:** delay instances of an output signal / further delay one or more of said delayed and down-converted input samples **Structure:** structure including "first delay module 2628," "second delay module 2630" shown in Fig 26, "delay module 3204" shown in Fig. 32 and described at 35:1-18; the sample and hold circuit 4501 and 4503 in Fig. 45 and described at 32:44-33:19; or an analog delay line having a combination of capacitors, inductors and/or resistors described at 35:19-27; or equivalents thereof.
PV: Plain and ordinary meaning

The parties' disputes here turn on the same questions of law as the disputes regarding the "down-convert and delay" terms above.

Whether § 112, ¶ 6 Applies. Intel demonstrated that § 112, ¶ 6 applies to both "delay module" terms because ***the claims*** fail to recite sufficiently definite structure to perform the claimed function. Intel Br. 7-9 (citing *Williamson*, 792 F.3d at 1351).

In response, PV does not dispute the claimed function, but again argues that disclosure of ***any*** related structure anywhere in the specification takes the "delay module" terms outside § 112, ¶ 6. Br. 13, 13 n.9 ("[T]hat a delay module uses *any* structure means … that § 112, ¶ 6 does *not* apply." (emphasis in original)). That is wrong as a matter of law, as underscored by the fact that PV (once again) ***cannot cite a single legal authority*** in support of its argument. Under controlling Federal Circuit precedent, the "critical question" regarding whether to construe a term as means-plus-function "is whether 'the claim term is ***used in common parlance*** [i.e., ***well-known***] or by persons of skill in the pertinent art to designate structure,' including either a ***particular*** [i.e., ***specific***] ***structure*** or a class of structures"—not merely "any" structure, as PV argues. *MTD Prods.*, 933 F.3d at 1341 (collecting cases). By arguing that disclosure of any structure takes a term outside of § 112, ¶ 6, PV is attempting to claim functionally—i.e., "delay module"—and then

cover all structures that could create delay—precisely what § 112, ¶ 6 prohibits. *Synchronoss Techs.*, 987 F.3d at 1367 ("It is not enough that a means-plus-function claim term correspond to every known way of achieving the claimed function; instead, the term must correspond to 'adequate' structure in the specification that a person of ordinary skill in the art would be able to recognize and associate with the corresponding function in the claim.").

The Corresponding Structure.[7] PV does not dispute the claimed function or the structures included in Intel's proposal, but again seeks to add black box "delay modules" from Figures 17, 19, and 23 to the construction. Br. 14. Here again, PV misperceives the law. As with the down-convert and delay terms, the structures that PV wants to include are improper not because they create "duplication" (Br. 14) but because they are empty. As Intel explained in its responsive brief, the specification states that these black box structures "can each be implemented using a switched capacitor topology 3204" ('706, 35:1-6), but the empty boxes themselves provide no structure. Intel Br. 9 n.8. Thus, the switched capacitor topology disclosed in the specification belongs in the claim construction (as Intel has proposed), but the empty black boxes do not.[8]

D. "harmonic", "harmonics"

Intel's construction tracks the '706 patent's express definition of "harmonic": "A harmonic is a sinusoidal component of a periodic wave. It has a frequency that is an integer multiple of the fundamental frequency of the periodic wave." '706, 9:39-47. PV contends the patent's definition should be modified to include "the fundamental frequency as the first harmonic." Br. 15. It should

[7] To narrow the disputes, Intel removed the phrase "that operates to delay sample/instances of a signal presented at its input by a known amount" from its proposed structure.

[8] PV argues for the first time in its reply (Br. 15) that the structure should include Figures 33A, 33B, and 34, which are already referred to in the specification passages included in Intel's construction. Intel does not object to including Figures 33A and 33B. Figure 34, however, is nothing more than a "delay module" containing a black box labeled "Analog Delay Line" and thus cannot be included.

not. *See Jack Guttman, Inc. v. Kopykake Enters., Inc.*, 302 F.3d 1352, 1360-61 (Fed. Cir. 2002) ("Where … the patentee has clearly defined a claim term, that definition usually is dispositive….").

First, PV wrongly accuses Intel of "purposefully omitt[ing]" the statement in the specification that "if the periodic waveform has a fundamental frequency of 'f' (also called the first harmonic), then it has harmonics at frequencies of 'n·f,' where 'n' is 2, 3, 4, etc." Br. 15-16 (citing '706, 9:39-47; '508, 9:53-61). But Intel both block quoted this language in its responsive brief and explained why it supported Intel's proposal: consistent with the object of the claimed inventions to up-convert a ***lower***-frequency signal to a ***higher***-frequency signal, this passage makes clear that the harmonics used in the claimed invention are "frequencies of 'n·f,' where 'n' is ***2, 3, 4, etc.***"—i.e., an ***integer multiple*** of the fundamental frequency that is at a ***higher*** frequency than the fundamental frequency. Intel Br. 12.

Second, PV points to portions of the specification, including 17:55-64 and Figure 19E, that recognize that the fundamental frequency may be referred to as a "harmonic" or the "first harmonic." Br. 16-17. PV's argument misses the point. Intel does not dispute that the fundamental frequency may, in some contexts, be referred to as the "first harmonic." But the question is how the patents use the word "harmonic[s]" in the specific context of performing the claimed invention's up-conversion. PV does not dispute that the transmitter patents are directed to up-conversion using harmonics. *See* Intel Br. 11; Br. 16-17. The purported invention works—i.e., there is up-conversion—***only*** if there is a difference in frequency between the input signal (which is at the fundamental frequency) and the harmonic that is output and used as the up-converted signal. Intel Br. 11. In that context, the "harmonic" must be at a higher frequency than the fundamental frequency. Consistent with that, the '508 patent specifically states—when discussing the Figure 19E, and in the very same passage on which PV relies—that "the harmonics" are "***up-***

converted representation[s]" of an input signal 1908 (i.e., the signal at the fundamental frequency). '508, 17:60-64.[9] In the context of the claimed up-conversion, therefore, "harmonic" does not include the underlying frequency of the input signal (i.e., the fundamental frequency).

PV's argument to the contrary—that the frequency of the harmonic could be at the ***same*** frequency as the input signal (i.e., the harmonic could be the "fundamental frequency")—would defeat the entire purpose of the invention. If the output harmonic is at the fundamental frequency, i.e., the same frequency as in the input signal, ***there would be no up-conversion***. '508, Abstract ("A method and system is described wherein a signal with a lower frequency is ***up-converted to a higher frequency***."); *see Ormco Corp. v. Align Tech., Inc.*, 498 F.3d 1307, 1313 (Fed. Cir. 2007) (term should be construed in way that "aligns with the patent's description of the invention").

Third, PV accuses Intel of "false[ly] recit[ing]" the relevant technology based on Intel's explanation that the "conversion from the sub-harmonic to the harmonic … constitutes the up-conversion." Br. 17. According to PV, "Up-conversion is <u>not</u> a conversion of a sub-harmonic to a harmonic." *Id.* (emphasis in original). But that argument directly contradicts the Abstract of the '508 patent, which states that "***[t]he*** up-conversion is accomplished by controlling a switch with an oscillating signal, the frequency of the oscillating signal being selected as a ***sub-harmonic*** of the desired output frequency" and that "the desired ***harmonic*** is output." '508, Abstract; *see also* Intel Br. 11; *infra* pp. 39-42 (control signal).

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[9] PV wrongly alleges that Intel omitted key language from this passage. Br. 16-17. As explained above, there is no dispute that the fundamental frequency (waveforms 1912a and 1914a in Figure 19E) can be referred to as the "first harmonic," and the patent uses that terminology here. *See* '508, 17:55-58. But the relevant passage for this claim term is the language Intel cited, explaining how "harmonics" relate to "up-conversion": "***the harmonics each represent an up-converted representation of signal 1908.***" *Id.*, 17:60-64. The only plausible reading of that language is that "harmonics" refers to harmonics at a higher frequency than the input signal. *See id.*, 11:5-7 ("***Up conversion:*** A process for performing frequency translation in which ***the final frequency is higher than the initial frequency***.").

It is PV that does not accurately describe the technology. PV states that "the up-conversion being referred in the specification is the up-conversion of a baseband signal to a transmission signal (for sending over the air)." Br. 17. PV is focused on the second of two primary embodiments, in which the invention is used as a transmitter and a low-frequency baseband information signal is ultimately transmitted at a higher RF frequency. PV suggests that up-conversion refers to the difference between the baseband frequency and the transmission frequency. But that cannot be correct because another embodiment involving up-conversion—the ***first*** embodiment identified in the patent's Abstract and described in the specification—involves neither a baseband signal nor a transmission signal. In this embodiment, "the higher frequency signal is used as a stable frequency and phase reference." '508, Abstract; *see id.*, 2:9-20, 9:59-61, 14:14-22. And the patent is clear that in ***both*** embodiments, the up-conversion is achieved—consistent with Intel's construction—by using a lower-frequency sub-harmonic signal to control a switch and thereby generate a higher-frequency harmonic signal:

> A method and system is described wherein a signal with a lower frequency is up-converted to a higher frequency. In one embodiment, the higher frequency signal is used as a stable frequency and phase reference. In another embodiment, the invention is used as a transmitter. The ***up-conversion is accomplished*** by controlling a switch with an oscillating signal, ***the frequency of the oscillating signal being selected as a sub-harmonic of the desired output frequency***. … In ***both embodiments***, the output of the switch is filtered, and the desired ***harmonic is output***.

Id., Abstract; *see id.*, 56:58-66 ("[T]he frequency of the oscillating signal that causes the switch in ***the present invention*** to open and close must be a 'sub-harmonic' of" the output frequency).[10]

E. "pulse widths that are established to improve energy transfer"

Claim 2 of the '706 patent requires that the pulse widths in the control signal be "established to improve" energy transfer in the down-conversion process. As Intel explained in its

[10] PV notes that the Jacksonville court included the "fundamental frequency" in its construction of "harmonic." Br. 15, 16. That decision is not controlling here and should be rejected.

responsive brief, this claim term is indefinite because neither the claim nor the specification describes ***what*** constitutes an improvement in "energy transfer," ***how*** to measure such improvement, and ***how much*** improvement is necessary to satisfy the claim term. Intel Br. 12-13.

PV's reply acknowledges but fails to address any of the questions that Intel raised regarding the scope of this claim term. Br. 18. For example, PV does not explain how a skilled artisan is supposed to measure the so-called improvement of energy transfer—by the amount of energy transferred? By the speed at which the energy is transferred? PV's brief fails to address Intel's questions for a simple reason—the patent provides no answers. The Federal Circuit has held that claims require "objective boundaries" that the '706 patent simply does not provide. *Interval Licensing LLC v. AOL, Inc.*, 766 F.3d 1364, 1373-74 (Fed. Cir. 2014). Indeed, similar claim language—"***improve*** a precision ratio"—has been found indefinite for exactly these reasons. *JobDiva, Inc. v. Monster Worldwide, Inc.*, 2014 WL 5034674, at *18 (S.D.N.Y. Oct. 3, 2014) (term "improve a precision ratio" indefinite, in part, because patent did not explain ***how*** to test improvement in precision ratio and no "standard test" was known to people of ordinary skill).

Absent any objective definition of "improving energy transfer" from the patent, PV and its expert attempt to invent a new meaning for the phrase, arguing that it refers to the use of "non-negligible apertures for energy transfer." Br. 18-19; Dkt. 43-1 [Steer Decl.] ¶¶24-31. This argument fails for at least two reasons. ***First***, PV clearly knew how to claim the use of non-negligible apertures, which are recited in multiple other claims. *See* '706, cls. 88, 91, 96, 109, 111. Thus, when PV used the more general, functional phrase "improve energy transfer," it must have meant something else (though it is unclear what). ***Second***, the only language that PV cites fails to support PV's construction. Br. 18-19; Dkt. 43-1 [Steer Decl.] ¶29. PV cites a single passage stating that the described pulse control mechanism will have non-negligible apertures and will "also"

improve energy transfer. '706, 32:9-18. But that merely provides an ***example*** of how to improve energy transfer, not a ***definition*** of that term.[11] Drafting a new quarterback might be one way to improve a football team, but it is not the ***definition*** of "improving a football team." PV does not and cannot provide any objective definition of "improve energy transfer" that is supported by the patent. The claim is therefore indefinite.

F. "means for under-sampling an input signal to produce an input sample of a down-converted image of said input signal"

Intel's Proposed Construction	PV's Proposed Construction
Function: under-sampling an input signal to produce an input sample of a down-converted image of said input signal and under-sampling the input signal according to a control signal **Structure:** the switch 2650 and the capacitor 2652 in Fig. 26 and described at 26:1-27:21, 28:20-28, and 39:25-28; the switch 5308 and capacitor 5310 in Fig. 53A and described at 28:46-47; the switch 5308 and capacitor 5310 in Fig. 53A-1 and described at 28:52-56 and equivalents thereof.	**Function:** under-sampling an input signal to produce an input sample of a down-converted image of the input signal and under-sampling the input signal according to a control signal **Structure:** switch 2650 in Fig. 26; switch 5308 in Figs. 53A/53A-1; and equivalents thereof

The parties dispute whether the required structure consists of both a switch and a capacitor (as Intel proposes) or a switch alone (as PV proposes). PV's reply arguments are without merit.

First, PV argues that Intel "shifts the focus from 'under-sampling' to down-converting" because (according to PV) only the switch is involved with under-sampling, while the capacitor is involved with down-converting. Br. 20. But it is the claim language itself that ties under-sampling to down-conversion. The claim specifically recites "***under-sampling*** an input signal ***to produce*** an input sample of a ***down-converted image*** of said input signal." PV attempts to ignore the "down-converted

[11] PV argues that there is no inconsistency between dependent claim 2 (which requires an "energy transfer" mode of sampling) and independent claim 1 (which requires the alternative "under-sampling" mode of sampling) because of the Court's construction of "under-samples" in the first case. Intel respectfully disagrees with that construction, given that the '706 patent defines under-sampling as the use of "negligible apertures that tend toward zero time in duration." '706, 1:6-12 (incorporating '551 patent); Dkt. 41-5 ['551 patent], 63:3-7.

image" language by focusing solely on the claim's "input sample" language. Br. 20 ("It does not say down-converting or under-sampling in order to down-convert. … [I]it says under-sampling to produce an input sample."). But PV disregards the claim language that directly follows "an input sample": "an input sample ***of a down-converted image***." One cannot under-sample to produce an input sample ***of a down-converted image*** without performing down-conversion. And as Intel explained in its responsive brief, both a switch ***and a capacitor*** are necessary to generate a down-converted signal. Intel Br. 14-17; '706, 29:18-22 ("When the switch 5308 is closed … charge is transferred from the input signal to the capacitor 5310. ***The charge stored during successive pulses forms down-converted output signal 5312***."); VDW Supp. ¶¶10-11, 17. PV's construction, which omits the capacitor, cannot be correct.[12]

Second, and in any event, PV's assertion that under-sampling requires only a switch (and not a capacitor) is wrong. PV's assertion is inconsistent with the '706 specification (through the incorporated '551 patent) which repeatedly describes ***under-sampling*** as requiring a capacitor (a/k/a holding module). *See, e.g.*, '551, 54:36-38 ("The under-sampling system 2701 includes a switch module 2702 ***and a holding module*** 2706."), 63:41-44 ("The under-sampling system 7802 includes a switching module 7806 ***and a holding module shown as a holding capacitance*** 7808."), 55:35-38 ("[T]he break-before-make under-sampling system 2401 under-samples the EM signal 1304 to down-convert it."), 56:19-21 ("The break-before-make under-sampling system 2401 includes a holding

[12] In an effort to evade the down-converting required by this claim term, PV argues that the "means for under-sampling" has two separate functions—"(1) under-sampling an input signal to produce an input sample of a down-converted image of the input signal and (2) under-sampling the input signal according to a control signal." Br. 19. According to PV, the second part does not require down-converting. But this is incorrect. The second part is a subset of the first: the second part specifies ***how*** the under-sampling is accomplished—"according to a control signal." Down-conversion is thus incorporated into both parts. In any event, the corresponding structure for the term must be sufficient to allow each part to be performed and therefore must include structure sufficient to down-convert. Moreover, since each part requires "under-sampling," and since, as explained here, under-sampling requires both a switch ***and*** a capacitor, the structure must include a capacitor. VDW Supp. ¶¶10-11, 17.

module 2416, which can be similar to the holding module 2706 in FIG. 27."). Indeed, sampling, as disclosed in the patent, necessarily requires a capacitor. A conventional RF receiver (such as those shown in Figure 1 of the '706 patent and Figure 11 of the incorporated '551 patent) may contain multiple switches that receive an input signal and that open and close based on a control signal but that, absent a capacitor, cannot create a "sample." VDW Supp. ¶11. Moreover, PV's assertion contradicts its prior representations to this Court. In the first case involving related patents (No. 20-cv-108), PV identified "key features" of under-sampling. No. 6:20-cv-108 (W.D. Tex.), Dkt. 51 at 5. Among those features, PV identified a "holding module"—which refers to a capacitor. *Id.* at 10 ("The capacitor is referred to as a 'holding' capacitor."). Thus, in the first case, PV acknowledged that a capacitor is a "key" part of under-sampling.[13]

Third, the single sentence from the patent specification on which PV relies (column 28:42-46, which refers to Figure 53A below) does not support its position. Br. 21.

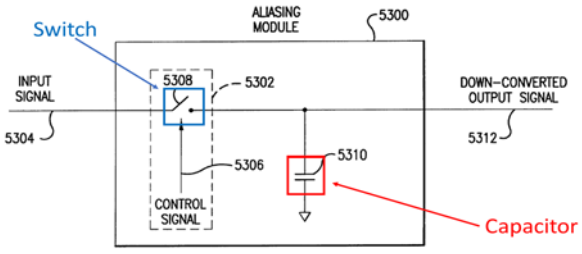


FIG. 53A

Intel explained in its responsive brief that PV misreads the sentence and that the specification clearly teaches that the aliasing module 5300 ***as a whole***—not just the switch (UFT module 5302) which is part of the aliasing module—performs under-sampling to produce an input sample of a

[13] PV argues that the structure should include columns 24:40-25:67 and 29:4-8. Br. 19. But as Intel explained, these sections describe various parts of Figures 15, 26, 27, 28, and 29 that are unrelated to the "under-sampling" function at issue. Intel Br. 16. Indeed, the fact that PV cites effectively the same passage (24:40-25:56) as relevant to the ***next*** term ("first delaying means") is further evidence that this passage is not clearly linked to the "means for under-sampling." Br. 23.

down-converted image of the input signal. Intel Br. 16-17. Indeed, since under-sampling is a form of aliasing (in the first case, PV even ***equated*** aliasing and under-sampling),[14] under-sampling is necessarily performed by the aliasing module, which includes a capacitor.

PV's only response is to assert that the "input sample" is somehow separate from the down-converted output signal 5312 and is produced solely by the switch. Br. 21. PV illustrates its assertion by annotating Figure 53A to show a blue arrow (which PV labels the "input sample of a down-converted image of the input signal") and an orange arrow (which PV labels as "the down-converted output signal"). Br. 21. But PV cites no evidence to support this alleged distinction. It is purely attorney argument and nowhere supported in the patent. As the only expert testimony addressing this issue confirms, the "down converted output signal" is the ***same*** signal as the one exiting the switch-capacitor pairing. VDW Supp. ¶¶12-16; '706, Fig. 53A.[15]

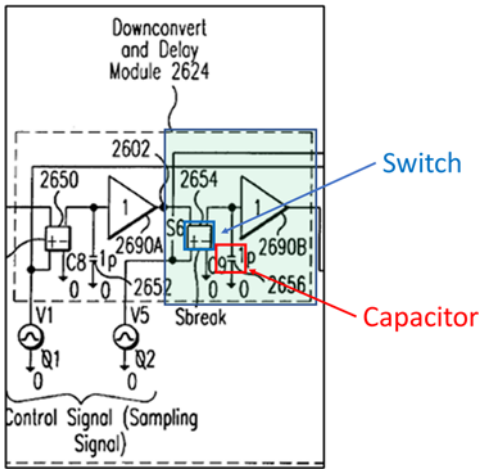
G. "first delaying means for delaying said input sample"

Intel's Proposed Construction	PV's Proposed Construction
Function: delaying said input sample **Structure:** the switch 2654 and capacitor 2656 shown in Fig. 26 and described at 25:57-27:21 and 28:20-28; and equivalents thereof.	**Function:** delaying the input sample of a down-converted image of said input signal **Structure:** capacitor 2656 in Fig. 26 of capacitor 5310 in Figs. 53A/53A-1; and equivalents thereof

[14] No. 6:20-cv-108 (W.D. Tex.), Dkt. 51 at 27 ("Under-sampling is the rate (referred to as an 'aliasing rate' in the patents) at which an input signal is sampled.").

[15] PV mistakenly claims Intel conceded that the capacitor is not involved in under-sampling when Intel stated, in its "first delaying means" argument, that the input sample would "transfer from the first switch." Br. 21 n.12. The input sample is formed by the interaction of the switch and capacitor and exists at the node adjacent to the switch and capacitor (the dot immediately above capacitor 5310). Intel accurately stated, as a shorthand in the context of discussing the timing of the sample's transmission through the circuit, that the sample will transfer "from the first switch"—i.e., from the node adjacent to the switch and capacitor—to the next circuit stage (the "first delaying means"). Intel Br. 18; Dkt. 41-9 [VDW] ¶86. PV's argument mistakenly suggests that the sample leaves the switch, goes down "through" the capacitor, and then another signal emerges and exits the circuit. But the sample is formed ***at the node*** by the interaction of the switch and capacitor. VDW Supp. ¶¶10-11.

PV's three reply brief arguments in support of its construction are wrong.[16] ***First***, PV wrongly argues that a capacitor alone (without a switch) performs the requisite "delay." Br. 22-23. As Intel explained, the "first delaying means" portion of the Downconvert and Delay Module 2624 consists of both switch (2654) and capacitor (2656). Intel Br. 17-19; '706, Fig. 26.



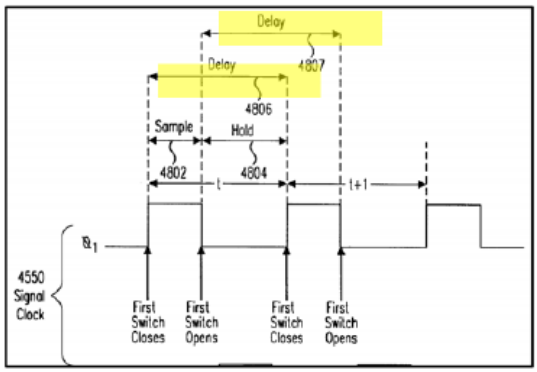
The patent explains that delays are accomplished by using a carefully calibrated set of switches and capacitors through which an input sample passes, as if on a conveyor belt. The timing of the signal's passage (and the corresponding delay of the signal) is dictated by clock signals that close and open the switches, allowing the capacitors to charge and discharge. '706, 26:25-30 ("At the rising edge of ϕ_2 at time t-1, a switch 2654 in the down-convert and delay module 2624 closes, allowing a capacitor 2656 to charge to the level of the capacitor 2652.").

PV asserts that only the capacitor is involved in creating the delay. It argues that "the specification equates 'holding' with delay," that the only device that can hold an input sample is a capacitor, and that the delay therefore "relates to *the time period* during which a capacitor is either charging up or holding energy." Br. 22-23. But PV ignores that this time period—the duration of the capacitor's charging and holding of energy—is dictated by the switch's opening and closing. *See id.*;

[16] PV also argues that Intel's function for "first delaying means" is improper (Br. 21), but Intel simply adopts the language recited in the operative claim.

'706, 27:1-6. In the figure above, for example, switch 2654 is timed to allow the capacitor to charge and discharge once during every clock cycle, creating a regulated delay of one-time unit. Without the switch, there would be no controllable delay of the input sample. Dkt. 41-9 [VDW] ¶86; VDW Supp. ¶¶19-23. Indeed, PV conceded in its opening brief that the switch dictates the timing of the capacitor's charging/discharging. PV Op. Br. 24-25 ("[T]he input sample (red arrow) is sent to capacitor 5310 where it is stored (delayed) until … the switch 5308 turns OFF (opens) and the switch [sic] discharges energy (orange arrow)."). It is thus the switch used in concert with the capacitor that creates the delay.

PV nevertheless asserts that this role of the switch in regulating the timing of the signal's progress "is *not* what the patent means by delay." Br. 22 (emphasis in original). But the same figure that PV cites (Figure 48) shows that the "delay" is ***defined*** by the opening and closing of the switch.



Delay period 4806 is shown as spanning a time that covers a sample period 4802 and a hold period 4804—with the delay period 4806 starting when "First Switch Closes" and ending when "First Switch Closes" again. '706, Fig. 48; *id.*, 34:16-59. The switch thus indisputably defines the period of the delay. This is underscored by the patent's description of "delay modules" (in Figure 48 and elsewhere) as specifically including a switch. *Id.*, 25:6-9 ("[T]he ***first and second delay modules*** 2628 and 2630 ***include switches*** that are controlled by a clock."); *see id.*, 34:60-62, 34:16-17, 32:61-66;

VDW Supp. ¶¶24-34.[17]

Second, PV argues that Figures 53A and 53A-1 should be included in the structure for the "first delaying means." They should not. These two figures are described as "illustrat[ing] an aliasing module 5300 (also called in this context a universal frequency down-conversion module) ***for down-conversion***," not for delay. *Id.*, 28:42-44. Claim 6 requires both (1) a "means for under-sampling an input signal to produce ***an input sample of a down-converted image*** of said input signal" (the preceding term), ***and*** (2) a "first delaying means ***for delaying said input sample***" (this term). Figures 53A and 53A-1 relate to the former, not the latter.

Third, PV argues that the structure should include columns 24:40-25:56. Br. 23-24. But this section of the specification describes various aspects of Figures 26, 27, 28, and 29 that are not directed to the function of "delaying said input sample." *See, e.g.*, '706, 24:58-59, 25:27-31. The section does not identify any additional ***structure*** for delaying the input sample.

H. "second delaying means for delaying instances of an output signal"

Intel's Proposed Construction	PV's Proposed Construction
Function: delaying instances of an output signal **Structure:** structure including "first delay module 2628," "second delay module 2630" shown in Fig 26 and described at 32:27-55, "delay module 3204" shown in Fig. 32 and described at 35:1-18; the sample and hold circuits 4501 and 4503 in Fig. 45 and described at 32:44-64; or an analog delay line having a combination of capacitors, inductors and/or resistors described at 35:19-27; and equivalents thereof.	**Function:** delaying instances of an output signal **Structure:** delay modules 1722A, 1722B, 1722C, etc. in FIG. 17; delay modules 1912, 1914 in Fig. 19; delay modules 2316, 2318 in Fig. 23; first delay module 2628, second delay module 2630 in Fig. 26; delay module 3204 shown in Fig. 32; sample and hold circuits 4501, 4503 shown in Fig. 45; analog delay line 3404 shown in Fig. 34 having a combination of capacitors, inductors, and/or resistors; and equivalents thereof

[17] PV mistakenly suggests that the switch merely "enables" the capacitor to perform the function and that such enablement does not make the switch part of the structure under *Asyst Techs.*, 268 F.3d at 1371. Br. 22. In *Asyst*, the enabling structure excluded from the structure was a wire (a communications line) between two operative components. By contrast, the switch here does not merely connect the capacitor to the upstream components but ***defines*** the delay function and is expressly described in the patent as being part of the delay module structure.

The dispute is whether the structure can include empty "black boxes" that encompass ***any*** circuitry that performs the claimed function (as PV contends). PV's arguments are wrong.

First, PV argues that delay module 1722 of Figure 17 is not merely an empty "black box" because the specification describes the switched capacitor topology 3204 of Figure 32 as "exemplary structure" for delay module 1722. Br. 24; *see* '706, 34:60-35:7. But that portion of the specification states that "delay modules [such as delay module 1722] … can be implemented using ***any apparatus or circuit*** that operates to delay an incoming signal by a predetermined amount." PV is not proposing to include black box 1722 ***as implemented with the actual circuitry*** (3204) that the patent discloses. Including delay module 1722—i.e., the box itself—as corresponding structure thus would effectively include as purported structure ***any configuration*** of circuitry that can perform the claimed function—precisely what § 112, ¶ 6 prohibits. *Supra* pp. 5-6; *see Noah Sys., Inc. v. Intuit Inc.*, 675 F.3d 1302, 1318 (Fed. Cir. 2012) (patentee gets benefit of functional claiming only by limiting the claim scope to the ***specific*** structures disclosed for performing the function).[18]

Second, PV fails to explain how 1912, 1914, 2316, 2318 and the analog delay line 3404 of Figure 34 are anything other than empty "black boxes." *See* Intel Br. 19-22; Br. 24-25. The patent provides no specific circuitry or structure and provides no indication of what is inside the box, how the box works, or how the box is supposed to perform the claimed function. These

[18] PV similarly contends that "***if*** the image of the switched capacitor topology 3204 of Figure 32 were included directly in delay modules of Figures 17, 19, 23, Figure [sic] 17, 19, 23 would be just like Figure 26," which the parties agree discloses sufficient structure. Br. 24. Yet PV fails to identify ***any*** disclosure linking the switched capacitor topology 3204 of Figure 32—even as "exemplary" structure—to the black box "delay modules" in Figures 19 and 23. *See* Br. 24; *see also Williamson*, 792 F.3d at 1351 ("Structure disclosed in the specification qualifies as corresponding structure if the intrinsic evidence ***clearly links*** or associates that structure to the function recited in the claims.").

black boxes thus cannot provide the requisite structure. *Bennett Marine, Inc. v. Lenco Marine, Inc.*, 549 F. App'x 947, 954 (Fed. Cir. 2013) (nonprecedential) (structure limited to "specific circuit shown in figure 2"; not "generic circuit shown in figure 1, i.e., any circuit fulfilling the required function").

Finally, PV argues, citing no authority, that "the physical inputs/outputs and which/how components are connected together are also part of the structure of circuits and their equivalents." Br. 25. But the fact that Figure 17 shows lines running in or out of delay modules 1722, which are themselves depicted as an empty box, is insufficient. *See Asyst Techs.*, 268 F.3d at 1370. PV offers no evidence or argument that the "physical inputs/outputs" to the black-box delay modules perform the agreed-upon function, i.e., delaying instances of an output signal.

I. "integral filter/frequency translator to filter and down-convert an input signal"

Proposed Constructions
Intel: **Function:** to filter and down-convert an input signal and to under-sample said input signal according to a control signal **Structure:** the Unified Downconvert and Filter (UDF) Module 2622 that includes: (1) the frequency translator 1108 having the down convert and delay module 2624; (2) a first delay module, including the delay module 2628 shown in Fig. 26, the delay module 3204 shown in Fig. 32 and described at 35:1-18, the sample and hold circuit 4501 or 4503 shown in Fig. 45 and described at 32:44-64, or the analog delay line having a combination of capacitors, inductors and/or resistors described at 35:19-27; (3) a second delay module including the delay module 2630 shown in Fig. 26, the delay module 3204 shown in Fig. 32 and described at 35:1-18, the sample and hold circuit 4501 or 4503 shown in Fig. 45 and described at 32:44-64, or the analog delay line having a combination of capacitors, inductors and/or resistors described at 35:19-27; (4) a first scaling module, including the first scaling module 2632 shown in Fig. 26, the resistor attenuator 3602 shown in Fig. 36 and described at 35:44-55, or the amplifier/attenuator 3704 implemented using operational amplifiers, transistors, or FETs shown in Fig. 37 and described at 35:60-67; (5) a second scaling module, including the second scaling module 2634 shown in Fig. 26, the resistor attenuator 3602 shown in Fig. 36 and described at 35:44-55, or the amplifier/attenuator 3704 implemented using the operational amplifiers, transistors, or FETs shown in Fig. 37 and described at 35:60-67; (6) a first adder including, the adder 2625 in Fig. 26, adder 1720 in Fig. 17, the adder 2522 in Fig. 25, the summer 3902 in Fig. 39, or the summer 4102 in Fig. 41; and

Proposed Constructions
(7) a second adder, including the adder 2626 in Fig. 26, adder 1720 in Fig. 17, the adder 2522 in Fig. 25, the summer 3902 in Fig. 39, and the summer 4102 in Fig. 41; and equivalents thereof. **PV:** "a circuit in which the input filtering operation is integrated with the frequency translation operation"

The parties dispute whether a term PV coined to describe its alleged invention—"integral filter/frequency translator"—should be construed under § 112, ¶ 6.

Whether § 112, ¶ 6 Applies. As Intel explained in its responsive brief, the '706 patent describes its alleged invention as an integrated filter and frequency translator, and the patent coined the term "integral filter/frequency translator" to describe that alleged invention. Intel Br. 23. Section 112, ¶ 6 applies to the term because claim 28 fails to disclose sufficient structure to perform the claimed function. The term "integral filter/frequency translator" appears only in claim 28 and is defined in terms of its function—which is "to filter and down-convert an input signal"[19]—and nothing in the intrinsic or extrinsic record suggests the term was "***used in common parlance*** or by persons of skill in the pertinent art to designate structure,' including either a ***particular structure*** or a class of structures." *See MTD Prods.*, 933 F.3d at 1341.

PV again seeks to avoid that straightforward conclusion by arguing that § 112, ¶ 6 does not apply if a term "connotes structure," and that because the '706 patent "relates to circuits, which have *physical* components," the term is not means-plus-function. Br. 26. But PV is unable to cite any law in support of its position because it is directly contradicted by the Federal Circuit precedent Intel cited above. *See Egenera*, 972 F.3d at 1374. PV's further argument that the claim term cannot be means-plus-function because Intel's expert identified various structures in the patent

[19] PV argues the function should include "under-samples [i.e., down-converts] said input signal according to a control signal." Br. 26 n.14. To narrow the disputes, Intel has added that language.

specification that are "used to create an 'integral filter/frequency translator'" (capacitors, inductors, resistors) (*see* Br. 26) demonstrates its complete misapprehension of means-plus-function law. ***Every*** means-plus-function claim must have corresponding structural components disclosed in the specification (and those elements must be included in the claim construction); otherwise the claim is invalid. *Biomedino*, 490 F.3d at 950 ("If there is no structure in the specification corresponding to the means-plus-function limitation in the claims, the claim will be found invalid as indefinite."). PV's argument would thus eliminate means plus function claiming.

The Corresponding Structure. PV takes issue with the number of words in Intel's proposed structure but does not contest even one word as being not clearly linked to the claimed function. Br. 25. Corresponding structure is corresponding structure under § 112, ¶ 6, no matter how many words it takes to describe it. PV cannot evade the limitations of means-plus-function by using functional claim terms like "integral filter/frequency translator" and then complaining that the patents—***which PV wrote***—describe many structures as performing the claimed function.

J. "modulated signal"

Intel showed in its responsive brief that its construction for "modulated signal" carefully tracks how the "Terminology" section in the '706 patent defines the term. Intel Br. 25. PV says this is "irrelevant" (Br. 26), but PV has not cited—in ***either*** of its briefs—***any*** part of the intrinsic record to support its proposal. Br. 26-27; PV Op. Br. 35-36. Instead, PV asks the Court to apply a construction for a different term in a different patent with a different specification, based on nothing more than attorney argument that the term "modulated signal" in the '706 patent is the same as the term "modulated carrier signal" in another. Br. 26-27. To do so would be serious error.

K. "filter tuning means for tuning one or more filter parameters"

The structure in Intel's proposed construction includes every component that the patent links to performing the claimed function. Specifically, Intel's construction includes the structures

that the specification discloses as "tunable." Intel Br. 26. PV's reply attacks Intel's construction as allegedly too narrow. According to PV, a filter parameter can be tuned not only using "tunable" components but also with "adjustable" components. PV thus seeks to add various "scaling modules" and "control signal generators" to the construction, which PV says are "adjustable." Br. 27-28. PV's argument fails.

First, PV cites no evidence from the specification for its assertion that filter parameters can be tuned using "adjustable" components. Nothing in the patent refers to "tuning" a filter parameter by using "adjustable" components generally, or by using the specific components that PV wishes to add to the construction. (Indeed, most of PV's components are not even identified as being "adjustable.") The ***only*** references to "tuning" in the specification relate to the ***tunable*** components that Intel has included in its construction. And tunable is not the same as adjustable: PV admits that "a 'tunable' component is merely ***one type*** of 'adjustable component.'" Br. 28.

Without ***any*** link—much less a clear link—between PV's proposed components and the required "tuning" function, those components cannot be included in the construction. "[S]tructure disclosed in the specification is 'corresponding' structure ***only if*** the specification or prosecution history ***clearly links*** or associates that structure to the function recited in the claim." *B. Braun Med., Inc. v. Abbott Labs.*, 124 F.3d 1419, 1424 (Fed. Cir. 1997). The Federal Circuit has applied this rule strictly because "[t]he duty of a patentee to clearly link or associate structure with the claimed function is the quid pro quo for allowing the patentee to express the claim in terms of function under section 112, paragraph 6." *Med. Instrumentation*, 344 F.3d at 1211. Indeed, even if a component disclosed in the specification is ***capable*** of performing the required function, it is not corresponding structure unless the patent makes a clear link between that component and the required function. *See Medtronic, Inc. v. Advanced Cardiovascular Sys., Inc.*, 248 F.3d 1303, 1312

(Fed. Cir. 2001) (ability to perform claimed function was "insufficient" to justify adding structure because "there is no clear link or association between the disclosed structure and the function recited in the means-plus-function claim limitation").

Second, PV misunderstands Intel's position regarding the scaling modules in Figures 17, 19, 23, 26, and 35. Br. 28-29. Those modules are (like so many of the structures that PV seeks to include in its claim construction) empty black boxes. Such a box without any known or disclosed components cannot provide the corresponding structure for a means-plus-function term. To be clear, a scaling module can be the required "filter tuning means," and Intel's claim construction expressly ***includes*** scaling modules—but they must have the structure of tunable components that is disclosed in the '706 patent for performing the tuning functionality. PV's attempt to include empty black boxes in the construction is a transparent attempt to broaden this means-plus-function claim beyond the disclosed structure and include structures that are not "tunable," and in fact, are not even "adjustable." Similarly, Intel agrees with PV that an "amplifier/attenuator" could be the required "filter tuning means." Br. 29. But the only such component disclosed in the patent is amplifier/attenuator 3704, which is depicted in Figure 37 as a black box, and the corresponding structure therefore must include the patent's disclosed structure (*e.g.*, operational amplifiers, transistors, or FETS) for performing the tuning function. *See* Intel Br. 27-28.

III. THE ASSERTED TRANSMITTER PATENTS

A. The '508 Patent

i. "pulse shaping means for shaping a string of pulses from a reference signal"

The parties dispute whether the structure of the "pulse shaping means" term can include "black boxes" that encompass any circuitry that performs the claimed function (as PV contends). Specifically, PV claims that the "harmonic enhancement module 4602" of Figure 46 discloses

sufficient structure based on the patent's statement that the module "is preferably comprised of digital logic devices." Br. 29-30 (citing '508, 47:3-7). PV contends that a "skilled person [would] know to use 'digital' and 'logic' devices as the structure instead of analog devices or circuity other than logic circuitry" and "to use a structure that produces the specific type of pulses disclosed in the specification." Br. 29-30. PV's argument fails for the following reasons.

First, PV again erroneously seeks to use the fact that the patent ties a black box (i.e., harmonic enhancement module 4602 in Figure 46) to one example of implementing the black box (i.e., "digital logic devices") to justify including the black box in the construction. Yet, as PV concedes, the "harmonic enhancement module 4602" shown in Figure 46 is not limited to "digital logic devices." Br. 29-30 (citing '508, 47:3-7 (module "is ***preferably*** comprised of digital logic devices")). PV's argument would allow it to cover ***any*** configuration for "pulse shaping" circuitry—an end-run around the means-plus-function bargain. *See supra* pp. 5-6.

Second, as Intel's expert Dr. van der Weide explained, "digital logic devices do not refer to unique structural components or arrangements." Dkt. 41-9 [VDW] ¶149. Rather, "[d]igital logic simply refers to a logic system rooted in binary code that *facilitates* the design of electrical circuits, but digital logic devices themselves are not specific, unambiguously constructed circuit components." *Id.* (emphasis in original). PV's expert, Dr. Michael Steer, does not dispute this characterization or explain otherwise: he merely notes that "digital logic devices are structural components and, for example, would be used in place of analog devices." Dkt. 43-1 [Steer Decl.] ¶33. Thus, neither PV nor its expert (nor the patent itself) provides definite structure that is clearly linked to performing the claimed function. *See, e.g.*, *Lufthansa Technik AG v. Astronics Advanced Elec. Sys. Corp.*, 711 F. App'x 638, 640-41 (Fed. Cir. 2017) (nonprecedential) (finding "control means" term indefinite for lack of adequate structure and rejecting claim construction defining

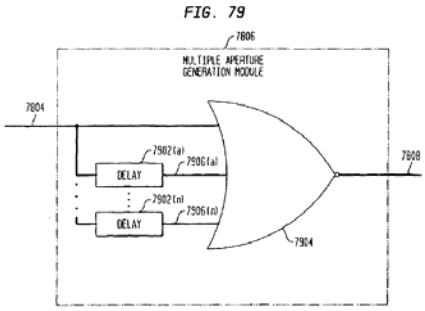
"control means" as involving "logic elements"; "[T]he '016 patent does not call out a specific, well-known component to perform the claimed function. Instead, the 'control means' refers to a nebulous set of logic functions within a black box that also performs other functions."); *Ergo Licensing, LLC v. CareFusion 303, Inc.*, 673 F.3d 1361, 1363-64 (Fed. Cir. 2012) (finding "control means" term indefinite for lack of adequate structure where specification disclosed only a "control device" as the corresponding structure).

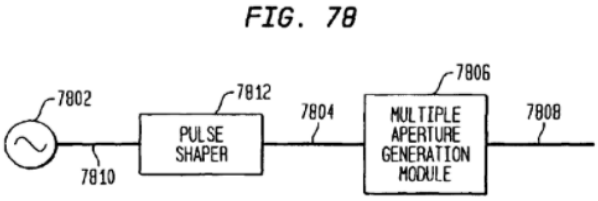
Finally, Intel did not "gloss over" the specification's description of "pulse shapers," as PV contends. Br. 30. To the contrary, as Intel explained, these passages refer only to empty "black boxes" and the functions they perform, not to any structure that can actually perform the required function. Intel Br. 33-34. PV's reply provides no evidence or argument otherwise.

ii. "aperture generation means … for generating a string of multiple pulses from said string of pulses"

Intel's Proposed Construction	PV's Proposed Construction
Function: generating a string of multiple pulses from said string of pulses **Structure:** the aperture generation module 7806 shown in Fig. 79 and described at 49:54-50:5; and equivalents thereof.	**Function:** generating a string of multiple pulses from said string of pulses **Structure:** aperture generation module 7806 in Fig. 78 having gate(s) and delay(s) such as the aperture generation module shown in Fig. 79; and equivalents thereof

The parties agree that the structure for this term includes aperture generation module 7806 in Figure 79, which shows actual circuitry for the module (as shown on the left below). The only dispute is whether the structure should also include aperture generation module 7806 in ***Figure 78***, where the module is depicted as an empty box (as shown on the right).





It should not, and each of PV's arguments is incorrect.

First, PV asserts that "Figure 78 is *not* empty" because "Figure 79 shows components of the 'multiple aperture generation module 7806.'" Br. 31 (emphasis in original). Intel agrees that Figure 79 does show the components of multiple aperture generation module 7806, and if PV's proposed structure were simply the multiple aperture generation module 7806 in Figure 78, ***as defined in Figure 79***, the parties would have no dispute. But PV is erroneously trying to stretch the structure to include not only the module with the components disclosed in Figure 79 but ***any module*** with any configuration of "gate(s) and delay(s)" that perform the recited function. Br. 31 ("What ParkerVision said was the structure should include gate(s) and delay(s) that perform the recited function (i.e., only those structures that perform the function)."). This amounts to an end-run around the means-plus-function bargain. *See Noah Sys.*, 675 F.3d at 1318. The patent discloses only ***one*** actual structure for performing the function—the structure disclosed in Figure 79. The term should therefore be limited to that structure and its equivalents. It would be legal error to permit PV to broaden the term with a construction that defines the structure as modules "***such as***" the module disclosed in Figure 79.

Second, PV is wrong that the specification's description of the aperture generation module undermines Intel's construction. PV cites column 49:54-56 for the proposition that the structure may include "*one* or more *delays*." Br. 31-32 (emphasis in original). But Intel's construction expressly cites this passage ("the aperture generation module 7806 … described at 49:54-50:5"), and

nothing in Figure 79 precludes the use of just one delay: Figure 79 shows an indeterminate number of delays (1 through *n*, where *n* could be 1).

Finally, PV is wrong that "Figure 78 ***itself*** provides structure"—i.e., structure independent of Figure 79. Br. 31 n.17. PV argues that the aperture generation module 7806 in Figure 78 is not empty and discloses structure because it has inputs and outputs. *Id.* But the fact that Figure 78 shows a line running into (and a line running out of) the empty "aperture generation module 7806" box does not suffice. As the Federal Circuit held in the only case that PV's brief cites, "[s]tructural features that do not actually perform the recited function do not constitute corresponding structure and thus do not serve as claim limitations." *Asyst Techs.*, 268 F.3d at 1370. In *Asyst*, for example, the Federal Circuit explained that "[a]n electrical outlet enables a toaster to work, but the outlet is not for that reason considered part of the toaster." *Id.* at 1371. Similarly, wires connecting the aperture generation module to other components may "enable" the module to work but do not perform the recited function ("generating a string of multiple pulses from said string of pulses").

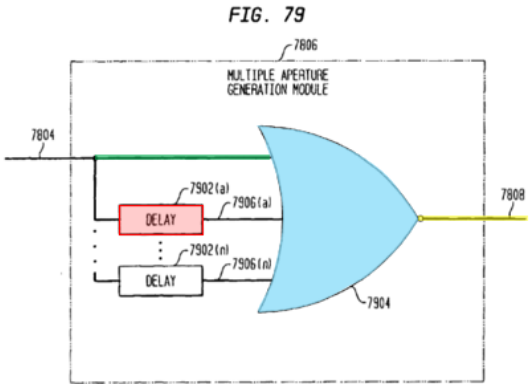
iii. "generating a string of multiple pulses from said string of pulses"

The parties dispute whether the word "multiple" in this term must be given meaning (as Intel contends) or whether it can be rendered meaningless by PV's "plain and ordinary" construction.

First, PV has no response to Intel's explanation that PV's "plain meaning" construction is an attempt to read the word "multiple" out of the claim. The claim recites the pulse shaping means to "shap[e] ***a string of pulses*** from a reference signal," and requires the "aperture generation means" to then "generat[e] ***a string of multiple pulses from said string of pulses***." '508, cl. 1; Intel Br. 36-37. PV agrees that the aperture generation means "receives the string of pulses" and "generates a string of ***multiple*** pulses … therefrom." Br. 38. But under PV's interpretation of this language, the "string of pulses" and the "string of ***multiple*** pulses" could be the same thing, i.e., any string with more than one pulse would satisfy both claim terms. PV's construction thus violates a fundamental rule of claim

construction by rendering the claim language "multiple" meaningless. *Comaper Corp. v. Antec, Inc.*, 596 F.3d 1343, 1348 (Fed. Cir. 2010) (declining to construe two terms as synonymous as "two different terms used in a patent have different meanings").

Second, PV is wrong that claim 3 of the '508 patent supports its proposed construction. Br. 39-40. Claim 3, which depends from claim 1, further requires that the "aperture generation means" comprise: (1) "logic gating means for outputting said string of pulses," and (2) "first delaying means for delaying said string of pulses for a first period of time." '508, cl. 3. Citing the "outputting said string of pulses" language, PV contends that claim 3 is directed to an embodiment where the aperture generation means merely outputs "the *same* string of pulses/number of pulses" that it receives. Br. 40 (emphasis in original). It does not. Figure 79 below illustrates the aperture generation module.



A string of pulses 7804 is input into aperture generation module 7806 and is then diverted along multiple lines before entering the NOR gate (7904 (blue)). '508, Fig. 79. In the topmost line (green), there is no delay, so the string of pulses may simply pass through the NOR gate (blue) and be output ***as the same string of pulses***. But the original string of pulses 7804 is also input to one or more delays (e.g., first delay 7902(a) (red)), which delay the pulses before being routed to the NOR gate (blue). *Id.*, Fig. 79, 49:54-50:5. The result is that the NOR gate "***outputs a string of multiple pulses*** 7808 that has a pulse [1] at every point in time that string of pulses 7804 has a pulse, ***and*** [2] at every point in time that first delayed string of pulses 7906(a) has a pulse." *Id.* The generation of this string with ***multiple***

the number of pulses as the original string of pulses tracks the language of claim 3: (1) the logic gating means (NOR gate 7904 (blue)) outputs the same "said string of pulses" that it receives, and (2) the "first delaying means" (7902(a), (red)) causes ***additional*** pulses to be output, thereby creating the string of multiple pulses required by claim 1. *Id.*, cl. 3, 49:54-50:5 (NOR gate "outputs a string of ***multiple*** pulses … ***having n+1 pulses for every cycle of string of pulses 7804***"); Fig. 80 (pulse train 8004 showing two pulses per cycle of string of pulses 7804), 50:6-11. Claim 3 therefore does not suggest claim 1 allows the output of only "the same string of pulses." VDW Supp. ¶¶38-41.

Third, PV incorrectly argues that the specification indicates that using a "higher amplitude signal"—that is, generating a signal with multiple the number of pulses as the string of pulses—"is merely a design consideration." Br. 40-41. The specification explains that the more the output signal is amplified as compared to the input signal (e.g., by using more pulses per cycle), the more the desired harmonic amplitude increases and the more the undesired harmonic amplitude decreases. Intel. Br. 38-39; '508, 50:37-40 ("[T]he desired harmonic amplitude is increased and the undesired harmonics decreased as a function of the number of pulses per cycle."), 50:23-49. By contrast, outputting the same string of pulses would have no purpose. '508, 50:38-41, 49:42-45 ("The purpose of using multiple apertures is because of the optimizing effect it has on the amplitude of the harmonic content of the output waveform."); VDW Supp. ¶37. Thus, the specification's statement that "[t]his increase in amplitude will be another consideration during the design of a transmitter" is referring to the ***magnitude*** of this increase in amplitude (e.g., whether to use four pulses per string rather than two), not to ***whether*** to increase the desired harmonic amplitude by using multiple pulses, which is expressly required by the claim. In any event, no argument based on the specification could justify what PV is attempting to do here: effectively rewriting the claim's specific requirement of "a string of ***multiple*** pulses." *Resonate Inc. v. Alteon Websystems, Inc.*, 338 F.3d 1360, 1364–65 (Fed. Cir. 2003).

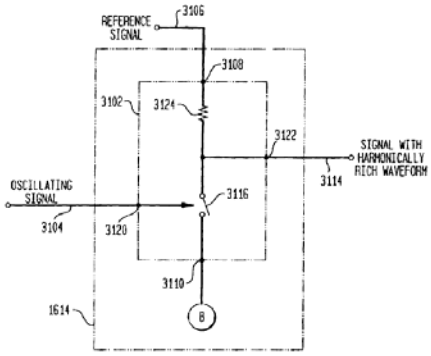
iv. "gating means for gating a bias signal under the control of said string of multiple pulses to generate a periodic signal having a plurality of harmonics at least one of which is at a desired frequency"

The parties dispute whether structures that do not gate a ***bias*** signal—i.e., those shown in Figures 31A, 32A, 33A, 55, 57C as gating a "***reference***" signal—should nonetheless be included as corresponding structure. They should not.

First, PV is flatly wrong to assert that Intel "ignore[ed]" portions of the specification identified by PV and had no response to PV's arguments regarding this term. Br. 33. Intel's responsive brief addressed PV's arguments in detail and explained how the patent distinguishes bias signals from reference signals, and how the portions of the specification PV cites consistently disclose gating a signal ***other than*** a bias signal. Intel Br. 48.

Second, PV does not dispute (because it cannot) that Figures 31A, 32A, and 33A explicitly show the gating of a "***reference*** signal":

FIG. 31A



E.g., '508, Fig. 31A. PV nevertheless argues that these figures are corresponding structure because the specification states that "reference signal 3106" may be "the summation" of an information signal 2702 with a bias signal 2704. Br. 33 (citing '508, 37:19-20). But the fact that the reference signal may be created in part from the bias signal does not make them the same signal. Instead, the cited passage—like the rest of the patent—specifically distinguishes the "reference signal 3106" (which is gated in these figures) from the "bias signal 2704" (which is not). Indeed, the passage states that the "reference

signal … may be the information signal 2702 ***by itself***" and thus could be ***wholly independent*** of a bias signal. *Id.* The patent includes multiple embodiments (e.g., Figure 28A) where a bias signal is gated. *See, e.g.*, '508, 34:34-35 ("A bias signal 2806 is gated as a result of the application of a modulated oscillating signal …."). Figures 31A, 32A, and 33A gate something different—a reference signal.

Third, PV's arguments regarding Figures 55 and 57C fail for similar reasons. PV again does not dispute that these figures show the gating of a "***reference*** signal" (Figure 55) or the gating of a signal generated by summing an "information signal" and a "bias signal" (Figure 57C), but argues that these figures constitute corresponding structure because, according to PV, "the bias signal is part of the combined signal" that is eventually gated. Br. 33. But, again, the signal that is gated is indisputably something other than a "***bias*** signal"—which is separately identified. The specification expressly states that the reference signal in Figure 55 may be the information signal itself and therefore would be entirely independent of any bias signal. '508, 60:32-34 ("It is well known to those skilled in the relevant art(s) that the information signal 5450 may be used as the reference signal 5506 without being combined with the bias signal 5422 ….").[20]

v. "gating"

The parties dispute whether "gating" requires a switch that opens and closes as dictated by "an independent control input" (as PV proposes).

First, PV contends that "gating" is limited to particular "switches" (and excludes diodes, which are not "dictated by an independent control input") because, for another disputed claim term ("gating means"), Intel identified only switches as corresponding structure. Br. 33-35. This is wrong. The term in dispute here is "gating." The "gating means" term in other claims is narrower:

[20] PV also argues that, because the Orlando court adopted PV's proposed construction, this Court should as well. Br. 32. But, as PV concedes, the decision in the Orlando court is not binding here. It should be rejected for the reasons explained above.

the parties agree it is a means-plus-function term and is therefore necessarily limited to the corresponding structure disclosed in the patent. *See supra* pp. 33-34. The only structure that the patent discloses as performing the specific function at issue in that claim—i.e., "gating ***a bias signal under the control of said string of multiple pulses to generate a periodic signal having a plurality of harmonics at least one of which is at a desired frequency***"—are particular switches. That fact, however, does not mean that the more general term "gating" is also so limited.

Second, as Intel explained, the specification does not support limiting "gating" to opening and closing a switch as "dictated by an independent control signal," because the patent specifically describes diodes—a type of switch with no separate "control input," much less an "independent" one. Intel Br. 44. In response, PV accuses Intel of "point[ing] to a *random* passage from the specification discussing diodes" because the cited portion of the specification (49:21-23) does not describe diodes as involved with gating. Br. 34 (emphasis in original). But PV admits that "gating is performed by a switch" (*id.*, 33), and the patent makes clear that a diode is a type of switch (*e.g.*, '551, 56:60-68), so a diode ***can*** perform gating. Intel cited the passage to show that diodes have no independent control input: the diodes referred to in that passage are shown in Figure 43 as "two-terminal devices that do not have any particular 'control input,' much less 'an independent control input.'" Intel Br. 44.[21] Intel's citation thus shows that a diode does not have a separate "independent control input," as PV's proposed construction requires.

Third, PV misunderstands Intel's criticism of PV's construction in yet another way. Intel's criticism of the "independent control input" aspect of PV's proposal was not, as PV suggests, simply

[21] PV also seeks to undermine Intel's reliance on the '551 patent because, PV claims, the '551 is not part of the '508 patent's family. Br. 34 n.19. This argument ignores that the '551 patent is ***explicitly incorporated by reference*** into the '508 patent and is thus intrinsic evidence. '508, 1:19-21; *see Cook Biotech Inc. v. Acell, Inc.*, 460 F.3d 1365, 1376-77, 1378 n.7 (Fed. Cir. 2006).

that the specification does use the "***exact phrase*** 'independent control input." Br. 35. Rather, as Intel explained, the patent contains ***no support whatsoever*** for such a requirement. *See* Intel Br. 44. The only supposed support that PV identifies in its reply brief—that claim 1 recites "gating means for gating a bias signal *under the control of said string of multiple pulses*" (Br. 35 (emphasis in original))—does not justify PV's construction. Intel does not dispute that gating will occur under the control of some signal, but there is nothing in patent that states that it has to be "an independent control input."

Finally, PV's brief again fails to support the "changing between the open and closed states of a switch" portion of its proposed construction. Intel noted in its responsive brief that PV's opening brief had not "cite[d] to any support for this language in its construction." Intel Br. 44. PV's reply again fails to offer evidence or argument justifying this portion of its construction.[22]

vi. "bias signal"

Proposed Constructions
Intel: "a signal having a fixed voltage or fixed current"
PV: "1) a signal having a steady, predetermined level; or 2) the modulating baseband signal"

The parties have two disputes regarding this term: (1) whether a bias signal has "a fixed voltage or fixed current" or rather "a steady, predetermined level", and (2) whether a bias signal can encompass "the modulating signal." PV's arguments fail on both issues.

First, PV is wrong to criticize Intel's construction as "not account[ing] for … the reality of how circuits actually work" because it refers to a "fixed" voltage or current. Br. 35-36. In its ongoing attempt to impugn Intel rather than focus on substance, PV accuses Intel of "carefully cho[osing] its 'fixed' language to be inflexible for non-infringement purposes." Br. 36. But "fixed"

[22] PV again notes that the Orlando court adopted PV's construction. Br. 33. But as PV concedes, that is not binding here. PV also notes that this Court "already addressed 'independent control input'" in other case before this Court (Br. 35), but that involved a different term, and as explained above, there is no basis to read "as dictated by an independent control input" into the term "gating."

comes directly from the patent—i.e., it is the word PV chose to use in its patent. '508, 34:34-60 ("The bias signal 2806 is generally a ***fixed*** voltage."), 33:22-23; '108, 32:11-13, 31:3-4. By contrast, PV's construction—"a signal having a steady, predetermined level"—is the after-the-fact creation of PV's lawyers and finds utterly no support in the patent. PV's construction is also unclear: it does not identify ***which*** of the many potential ***parameters*** of the signal—e.g., voltage, current, frequency, amplitude etc.—must be set at a "steady, predetermined level." Claim construction is supposed to define and clarify terms to assist the fact finder. *See O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1362 (Fed. Cir. 2008). By adding new ambiguities, PV's construction does the opposite.

Second, PV is wrong that a "bias signal" can be a "modulating baseband signal"—which is the precise opposite of the "steady, predetermined" signal described in the first portion of PV's construction. Br. 36-38. PV's proposed construction—defining a bias signal as a steady, predetermined signal or as modulating signal that varies—is internally inconsistent and effectively renders the term meaningless. PV's attempt to overcome this badly misreads the patent specification. PV expresses its argument as a three-part syllogism: [1] the bias signal can be the "information signal," [2] "the 'information signal' is a 'modulating baseband signal,'" so [3] "the 'bias signal' can also be a 'modulating baseband signal.'" Br. 37. There is no dispute about proposition #2: the patents clearly define an "information signal" as including a "modulating baseband signal." *See, e.g.*, '508, 10:12-18. PV's logic fails, however, because proposition #1 is wrong: the bias signal ***cannot*** be the information signal.

Nothing in the '508 or '108 patents support PV's proposition #1 (that the bias signal can be a varying information signal). As Intel explained in its opening brief, reference signals vary (because they may be the information signal or be the sum of the information signal and a bias

signal), but bias signals do not vary. Intel Br. 45-46. PV states that "it is well known" that the bias signal can be the information signal, but PV's ***only*** citation for that argument is the same sentence that Intel explained in its responsive brief: "the information signal 5650 may be used as the bias/reference signal 5646 directly without being summed with a bias signal." '508, 61:14-17. As Intel explained, the phrase "bias/reference signal 5646" is used merely as a shorthand for the location in Figure 56 where the gated signal is either a bias signal or a reference signal, depending on the mode. Intel Br. 47-48. That sentence is plainly referring to the AM mode where the information signal is used as a ***reference signal***. '508, 59:13-15 ("Typically, in the AM mode, ***this bias/reference signal is referred to as the reference signal to distinguish it from the bias signal*** used in the FM and PM modes."). Indeed, the patents clearly and consistently distinguish the bias signal from the reference signal based on the bias signal's unvarying nature:

- "In the FM and PM modes, ***bias/reference signal 5308 is preferably a non-varying signal, often referred to simply as the bias signal***." '508, 59:4-6.
- "In the FM and PM modulation modes, bias/reference signal 5646 is ***referred to as a bias signal 5646, and it is substantially non-varying***. In the AM modulation mode, an information signal 5650 may be combined with the bias signal to create what is referred to as the reference signal 5646." '108, 56:1-27.

PV nevertheless asserts that the information signal alone can be a bias signal (not a reference signal) because "[w]hen only an information signal is used, a reference signal is *never* created (because the combination of the bias and information signal never occurs)." Br. 37 (emphasis in original). But PV's assertion is directly contradicted by the patents:

> In one embodiment of the invention, the reference signal is created by combining the information signal 4502 with a bias signal. ***In another embodiment of the invention, the reference signal is comprised of only the information signal 4502***.

'508, 23:27-31; *see also id.*, 38:3-6 ("Generally, ***the reference signal 3106*** is a function of the information signal 2702, and may either be the summation of the information signal 2702 with a bias signal or it ***may be the information signal 2702 by itself***."), 60:32-34 ("It is well known to

those skilled in the relevant art(s) that ***the information signal 5450 may be used as the reference signal 5506 without being combined with the bias signal 5422*** ….").[23]

B. '108 Patent

i. "control signal"

Proposed Constructions
Intel: "an oscillating signal that controls the first switch with a frequency that is a sub-harmonic of and lower than the desired output frequency" **PV:** Plain and ordinary meaning

PV argues that Intel's proposed construction limits the term "control signal" to a particular embodiment of the specification. Br. 41. This is wrong. Intel's construction reflects the fact that ***every*** embodiment in the '108 patent up-converts by using a control signal to control a switch that generates a harmonically rich signal and then by selecting one of the higher-frequency harmonics as the up-converted signal. PV, on the other hand, by advocating for an interpretation of "control signal" that would include virtually any electrical or electronic input, is reading the alleged invention of the '108 patent out of the claims. PV's reply arguments fail for three primary reasons.

First, PV cites the patent's definition of the phrase "control a switch" and notes the definition's language that a switch is typically "controlled by an electrical or electronic input." Br. 41 (citing '108, 7:57-64). That general statement is not in dispute. But that statement does nothing to answer the question of what ***type*** of "electrical or electronic input"—i.e., what "control signal"—the '108 patent uses to up-convert, as required by the claim. The Abstract and the Summary of the Invention of the '108 patent make that clear: "The up-conversion is accomplished by controlling a switch with an oscillating signal, the frequency of the oscillating signal being

[23] PV argues that because the Orlando court adopted PV's proposed construction, this Court should as well. But the decision in the Orlando court is not binding, and Intel respectfully submits that the Orlando court got it wrong. Federal Circuit precedent—which is binding and requires terms to be construed in light of the patent specification—compels the opposite conclusion.

selected as a sub-harmonic of the desired output frequency." '108, Abstract; *id.*, 2:9-41.

Second, PV's only substantive response to Intel's detailed explanation of the '108 patent's purported invention is to argue that the cited specification passages refer merely to specific embodiments, not the invention as a whole. Br. 41-42. PV appears to believe that because these passages use the word "embodiment," every aspect of what is described is optional and the patent says nothing about the type of control signal that must be used. This is wrong.

As Intel explained in its responsive brief, up-conversion was well known long before PV filed its '108 patent (*see, e.g.*, '108, 14:1-6), and the patent therefore describes a purportedly new ***method*** of up-conversion: using a particular type of control signal to up-convert an information signal. Specifically, the patent describes that the control signal must be a sub-harmonic of the desired output frequency. *Id.*, 2:19-23 (Summary of the Invention). That control signal controls a switch that generates a harmonically rich signal, consisting of harmonics having frequencies that are integer multiples of the control signal. *Id.*, 16:24-28. The system then selects one of these higher-frequency harmonics and uses that as the up converted signal. *Id.*, Abstract ("[T]he output of the switch is filtered, and the desired harmonic is output.").

Consistent with the Abstract and Summary of the Invention, ***every*** embodiment in the '108 patent up-converts by using this particular control signal (i.e., a signal that is a sub-harmonic of and lower than the desired output signal) to control a switch that generates a harmonically rich signal from which a higher-frequency harmonic is drawn. That each of the different applications of the invention are described as embodiments does not permit PV to disregard the core idea underlying all of them: up-converting by controlling a switch using a control signal with a frequency that is a sub-harmonic of and lower than the desired output frequency. For example, PV points to language in the Abstract of the '108 patent that refers to two "embodiments." Br. 41-42.

But the language that Intel relies on (highlighted in green in PV's brief) plainly applies to "[t]he up-conversion" in both embodiments: "***The up-conversion***"—i.e., the up-conversion of the claimed method and system described in the first sentence of the abstract—"***is accomplished*** by controlling a switch with an oscillating signal, the frequency of the oscillating signal being selected as a sub-harmonic of the desired output frequency." '108, Abstract.

Similarly, PV criticizes Intel's citation of column 52:2-9 ("the frequency of the oscillating signal that causes the switch in the present invention to open and close must be a 'sub-harmonic' of 900 MHz [the desired frequency of the transmitted signal]") because the cited paragraph begins: "As described in the ***example*** above." Br. 42. This passage is undoubtedly an "example," but it is an example that confirms Intel's point: the passage is explaining how to apply PV's alleged invention to achieve a specific (900 MHz) output—"the frequency of the oscillating signal … must be a 'sub-harmonic' of 900 MHz."

The same is true for each of PV's other arguments. Br. 42. PV notes, for example, that column 9:50-61 refers to one of the two main embodiments of the patent (the phase comparator/frequency comparator embodiment, rather than the transmitter embodiment), but PV ignores the broader, more general language in this same passage, which is taken from the "Overview of the Invention" section and which describes how "***the present invention***" takes "advantage of the relatively low cost of low frequency oscillators to generate stable, high frequency signals." Moreover, the other main embodiment—the transmitter embodiment—also describes using a low-frequency control signal to generate harmonics in order to up-convert, just like the other embodiments in the '108 patent. '108, 15:46, 16:24-36. Similarly, the other embodiments that PV cites include various features that are unrelated to the frequency of the control signal and thus do not undermine Intel's proposed construction. *See, e.g.*, *id.*, 16:24-28

(describing same invention using a ***frequency modulation mode*** (as opposed to a phase or amplitude modulation mode)).

Intel's proposed construction of "control signal"—"an oscillating signal that controls the first switch with a frequency that is a sub-harmonic of and lower than the desired output frequency"—faithfully captures the invention and describes the only type of control signal described in the patent for performing up-conversion. PV's "plain and ordinary meaning" interpretation, by contrast, would place no limits on the type of control signal used, would read the purported invention out of the claims, and would cover prior-art systems for up-conversion that the patent purports to improve upon. PV's construction violates the fundamental rule of claim construction that terms must be construed in light of the specification. *See Apple Computer, Inc. v. Articulate Sys., Inc.*, 234 F.3d 14, 25 (Fed. Cir. 2000) ("the claim must be interpreted in light of the teachings of the written description and purpose of the invention described therein.").

ii. "third switch"

Proposed Constructions
Intel: "a switch controlling whether the antenna transmits said signal"
PV: Plain and ordinary meaning, or "switch" as construed by the Court in Case No. 6:20-cv-108

PV criticizes Intel's proposed construction because it requires the third switch to ***control*** whether the antenna transmits the signal. Br. 43. PV's argument relies on one portion of a sentence in the specification, which states that "R/T switch 5406"—which corresponds to the third switch in claim 1—"***connects*** the transmission signal to the antenna 5402." '108, 55:23-25. The third switch does connect the transmission signal to the antenna, but PV's argument ignores both the rest of the sentence and the surrounding context, which make clear that, by virtue of this connection, the third switch controls whether the antenna transmits the signal.

The patent describes using a "half duplex" system, which uses a single antenna that can

"***either transmit or receive***, but cannot do both simultaneously." '108, 49:62-64. The "third switch" (called the "R/T switch" in the specification) is tasked with controlling whether the system is in transmit mode or receive mode. *Id.*, 55:5:25, 54:30-58, 55:46-48, 54:39-43. When the third switch connects the signal to the antenna (i.e., the switch is closed), the system is in transmit mode and the signal can be transmitted by the antenna. *Id.* When the third switch does not connect the signal to the antenna (i.e., it is open), the system is in receive mode and the signal cannot be transmitted by the antenna. *Id.*, 54:39-43. The third switch thus indisputably controls whether the antenna transmits the signal. When understood in this context, the ***complete*** text of the sentence from which PV quotes shows that the third switch controls the transmit function by virtue of its ability to connect the signal to the antenna: "***because the transceiver is performing the transmit function***, R/T switch 5406 ***connects*** the transmission signal to the antenna 5402." *Id.*, 55:23-25.[24]

The connection between the third switch and the antenna, in other words, is a connection that controls whether the antenna transmits the signal, not merely any connection between two circuit components. As Intel explained (Intel Br. 58), interpreting "third switch" to cover any physical connection between a switch and the antenna—including indirect connections—would render the "third switch" claim language meaningless. Every component in a circuit is arguably connected to every other component through intermediate components. PV's "plain meaning" interpretation therefore would cover ***any*** switch in the system and would fail to differentiate the "third switch" in claim 1 from the other switches in the claim (i.e., the "first switch" that

[24] PV further argues that "Intel improperly seeks to limit a structural component to a purpose." Br. 43. To the contrary, Intel's construction defines "third switch" consistent with its ***function***—controlling whether the antenna transmits a signal. In its responsive brief, Intel explained that the Federal Circuit has held that it is "entirely proper to consider the functions of an invention in seeking to determine the meaning of particular claim language." *Medrad, Inc. v. MRI Devices Corp.*, 401 F.3d 1313, 1318-19 (Fed. Cir. 2005). PV's reply brief offers no response.

upconverts, or the "second switch" that routes the signal to the frequency conversion module).[25]

iii. "pulse shaper"

Proposed Constructions
Intel: "a circuit configured to enhance a desired harmonic by shaping an oscillating signal"
PV: "circuitry that shapes an oscillating signal to generate a string of pulses"

PV modified its proposed construction of "pulse shaper" in its reply brief to include the function of "shap[ing] an oscillating signal," consistent with Intel's construction and the specification. The parties' remaining dispute is whether the term should be further defined as it is defined in the specification—as enhancing a desired harmonic (as Intel proposes).

PV argues that Intel's construction should be rejected because "pulse shaping is not always equated with harmonic enhancement." Br. 44. That is wrong. The patent plainly equates pulse shaping with harmonic enhancement:

- "Harmonic enhancement may also be called 'pulse shaping' since the purpose is to shape the oscillating signal 2804 into a string of pulses of a desired pulse width." '108, 42:21-23.
- "The harmonic enhancement module (HEM) 4602 (Fig. 46) is also referred to as a 'pulse shaper.'" *Id.*, 42:49-50.
- "In this first embodiment of a harmonic enhancement module 4602, herein after referred to as a pulse shaping circuit 4602 …." *Id.*, 43:54-57.

This makes sense because harmonic enhancement is the expressly stated purpose and result of "shaping the oscillating signal" as described in the patent. *Id.*, 42:19-29. Pulse shaping ensures that the oscillating signal is "crisp" so that the switch—which is downstream of the pulse shaper and controlled by the oscillating signal—will generate a "harmonically rich signal" and "each of the

[25] PV also argues that "[i]nserting Intel's construction of 'third switch' into claim 12 would lead to a nonsensical result." Br. 43. But as explained in Intel's responsive brief, the fact that claim 12 reverses the numerical labels for the switches does nothing to undermine Intel's construction for claim 1. Intel Br. 58 n.25. PV's brief offers no response.

harmonics … will have the information modulated on it." *Id.*, 42:14-18; *see id.*, 43:17-26.

PV's specification citations do nothing to undermine Intel's construction. Br. 44, 45. For example, the specification's statement that "some embodiments of the invention include harmonic enhancement, whereas other embodiments do not" ('108, 39:56-57) does not indicate that pulse shaping is different from harmonic enhancement. Rather, it merely states that a pulse shaper (i.e., harmonic enhancement module) may not be used in every embodiment. That is confirmed by the patent's explanation that "harmonic enhancement may be needed in ***some*** embodiments" (*id.*, 42:20-21), while stating in the very next sentence that harmonic enhancement is the same as pulse shaping: "***Harmonic enhancement may also be called 'pulse shaping'*** …." *Id.*, 42:21-22. None of PV's citations creates any daylight between pulse shaping and harmonic enhancement.

Finally, PV alleges that Intel has been inconsistent by construing "pulse shaper" in the '108 patent to refer to harmonic enhancement, while construing "pulse shaping means" in the '508 patent without including the "harmonic enhancement modules" in Figures 46, 51B, and 51C of the '508 patent. Br. 44. There is no inconsistency. Intel did not include those "harmonic enhancement modules" in the '508 construction only because—consistent with settled means-plus-function precedent—those modules are empty black boxes that fail to disclose any structure for performing the claimed function of the means-plus-function term. Nothing in Intel's construction suggests that pulse shaping is ever anything other than harmonic enhancement.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that all counsel of record are being served with a copy of the foregoing document via the Court's CM/ECF system per Local Civil Rule CV-5(b)(1) on May 12, 2021.

/s/ J. Stephen Ravel
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