PVL2520R

Dual-Band Low Noise Amplifier

The PVL2520R is a dual-band low noise amplifier with integrated bypass mode. The LNA features high linearity and low noise amplification achieving high dynamic range for demanding applications such as CDMA and EVDO downlink.

The PVL2520R helps provide a space saving and cost effective solution for high performance receivers.

The device is easily controllable with a two wire interface to set low band (LB) and high band (HB) modes of operation as well as bypass mode. In bypass mode, the device has no current demand (0 mA).

General Features

- Operating RF Frequency:
  - LB : 800 MHz to 920 MHz
  - HB: 1700MHz to 2000MHz
- Excellent Linearity
  - IIP3HB=+15dBm
  - IIP3LB=+8.5dBm
- Bypass Mode
  - IIP3HB=+25dBm
  - IIP3LB=+26dBm
- Low Noise Figure
  - NFLB=1.35dB
  - NFHB=1.8dB
- Low power consumption
- Small PCB area requirement
- Low external component count
- Temp range: -40 to +85 °C

Applications

- Cellular
- Wireless Infrastructure
- Small Cell

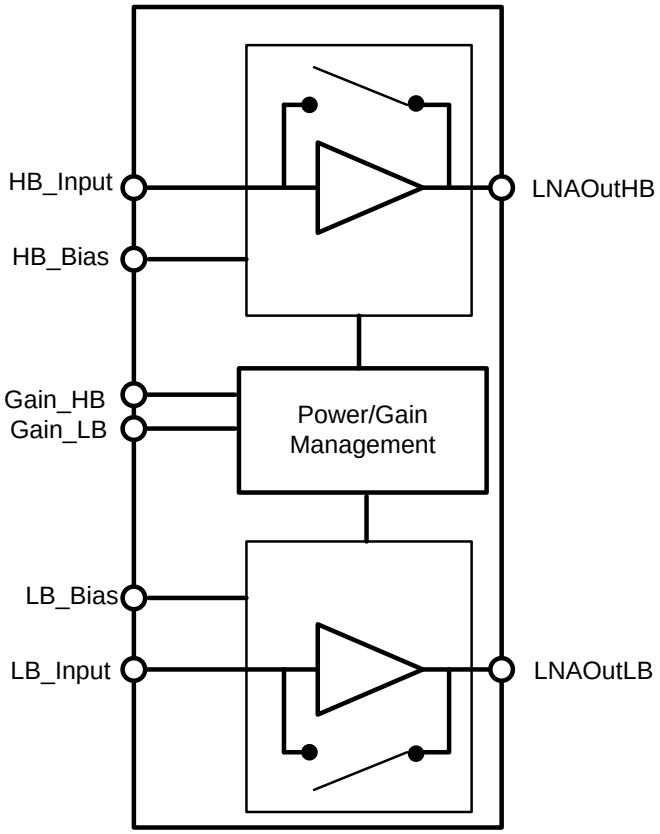


Figure 1: Functional Block Diagram

Contents

General Features 1

Applications 1

Figure 1: Functional Block Diagram 1

Pin Description 3

Figure 2: PVL2520R Pin Connections 3

Absolute Minimum and Maximum Operating Conditions 4

Electrical Specifications / Recommended Operating Range 4

Application Information 6

Overview 6

Gain Modes 6

Noise Figure and Gain 6

Decoupling 6

Inter-Stage Match 6

Figure 3: Application Schematic 7

Bill of Materials – Evaluation Board 8

Mechanical Information 9

Dimensions and Pad Locations 9

Die Image 12

Pin Description

Pin Number	Pin Name	Description	Side
A1 (pin1)	VEE	Ground	
A4	NC	No connection	
A6	VEE (Ring)	Ground	
B1	RF OUT LB	Low Band RF Output	
B7	NC	No connection	
C1	VCC	Power Supply Voltage Connection	
C3	VCC	Power Supply Voltage Connection	
D1	RF OUT HB	High Band RF Output	
E1	VEE	Ground	
E3	EM HB	High Band RF Ground	
E6	EM LB	Low Band RF Ground	
E7	Gain LB	Low Band Gain Control Mode	
F1	Bias HB	High Band Bias Connection	
F2	RF IN HB	High Band RF Input	
F3	VEE	Ground	
F4	Bias LB	Low Band Bias Connection	
F5	RF IN LB	Low Band RF Input	
F6	VEE	Ground	
F7	Gain HB	High Band Gain Control Mode	

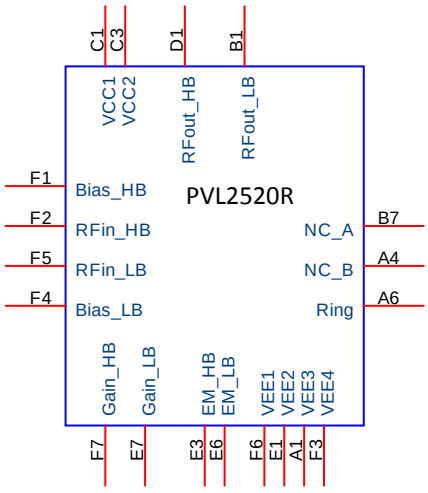


Figure 2: PVL2520R Pin Connections

Absolute Minimum and Maximum Operating Conditions

Parameter	Symbol	Conditions	Min	Max	Unit
PVL2520R Supply Voltage(s)	All V_{CC}	Pins C1,C3	-0.3	+3.6	V
Storage Temp			-40	+140	° C
Low or High Band Select	Gain_HB, Gain_LB	Pins E7,F7		VCC+0.3	V
RF Inputs		Pins F2,F5		-1	dBm

Electrical Specifications / Recommended Operating Range

(Tc = +25 ° C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	Pins C1,C3	+2.5		+3.3	V
Power Supply Current	Icc					
Low Band				9		mA
High Band				9		mA
Gain/Bypass Mode	Gain_HB, Gain_LB	LNA max gain	+2.25	VCC		V
		LNA bypass	0		+0.5	V
RF Output Frequency						
Low Band			800		920	MHz
High Band			1700		2000	MHz
Power Gain						
Low Band	High Gain Mode	Vcc=+3Vdc		+14		dB
	Bypass Mode			-4.5		dB
High Band	High Gain Mode	Vcc=+3Vdc		+12		dB
	Bypass Mode			-4.5		dB
Noise Figure						
Low Band		Vcc=+2.5V		1.35		dB
		Vcc=+3.0V		1.5		dB
High Band		Vcc=+2.5V		1.8		dB
		Vcc=+3.0V		1.9		dB
Noise Figure						
Low Band	Bypass Mode			5		dB
High Band	Bypass Mode			5		dB
Third Order Intercept						
Low Band	IIP3 High Gain Mode	Vcc=+2.5V		+8.2		dBm
		Vcc=+3.0V		+8.9		dBm
High Band	IIP3 High Gain Mode	Vcc=+2.5V		+14		dBm
		Vcc=+3.0V		+15		dBm
Third Order Intercept						
Low Band	IIP3 Bypass Mode			+25		dBm
High Band	IIP3 Bypass Mode			+26		dBm
Input Compression	ICP	Low and High Bands	-2			dBm

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Isolation Low Band High Band	S12			 24 21		 dB dB
Input Return Loss	S11	Low and High Bands		12		dB
Output Return Loss	S22	Low and High Bands		12		dB
Operating Temp			-40		+85	° C

Application Information

Overview

A typical applications schematic is shown below in figure 2. This circuit is configured with matching and decoupling components for a dual band solution. “Place holders” for matching elements are shown to allow optimal matching between the PVL2520R and interface devices. Depending on printed circuit board layout and application, these elements may be omitted.

Gain Modes

Two pins are provided for LNA gain modes. The low band and high band LNA’s can be independently controlled. A logic “high” applied to Gain_HB and/or Gain_LB places the LNA’s in high gain / normal operation mode. A logic “low” applied to Gain_HB and/or Gain_LB places the LNA’s in bypass mode. In bypass mode, maximum linearity is achieved while no dc current is consumed.

Noise Figure and Gain

Noise figure and gain can be optimized through modification of the input match. If L5 is increased to 15nH, the cell-band gain will increase about 0.5dB with a slight degradation in noise figure. The evaluation board is configured for good noise figure while keeping the cell-band gain at approximately 14dB. Similar tradeoffs can be made through modification of the pcs-band input match.

Decoupling

Power supply decoupling is achieved with ceramic capacitors placed close to the power supply pins. The values shown provide adequate decoupling. Some of the decoupling capacitors may be removed depending on the application and PCB layout.

Inter-Stage Match

The input and output impedance matching circuits can significantly influence performance. Actual interface matching values should be selected based on PCB layout as well as optimization of linearity, noise figure, and return loss.

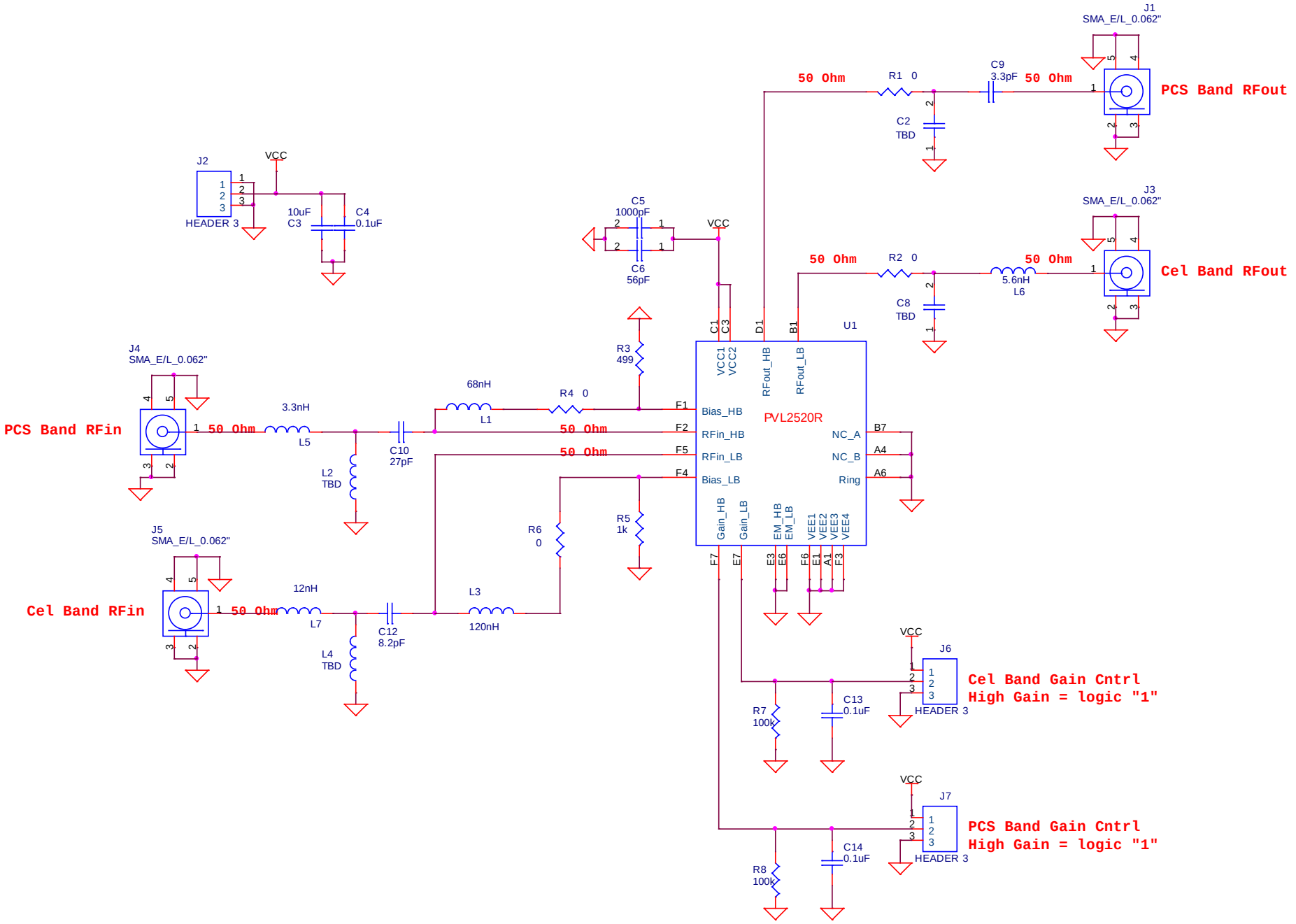


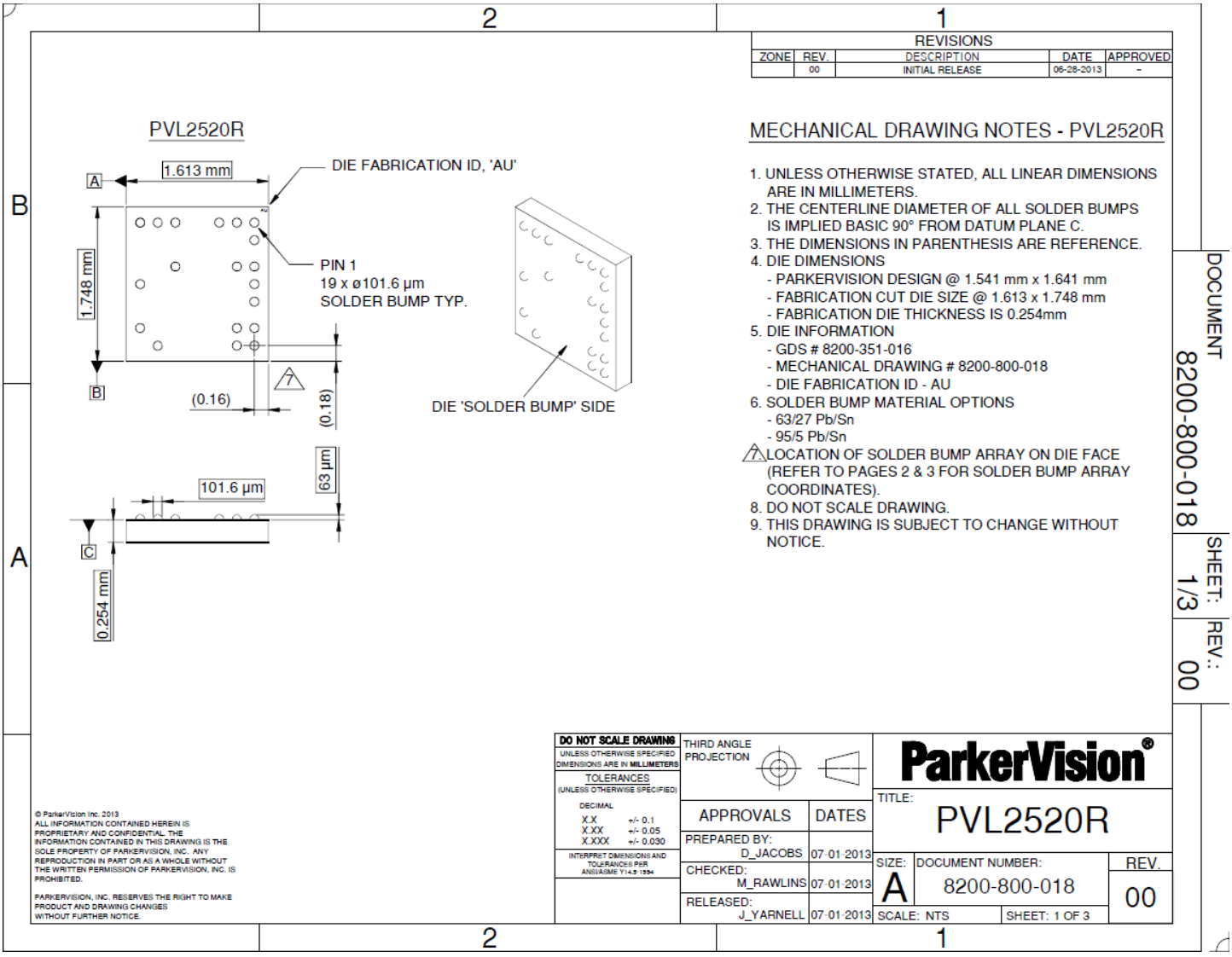
Figure 3: Application Schematic

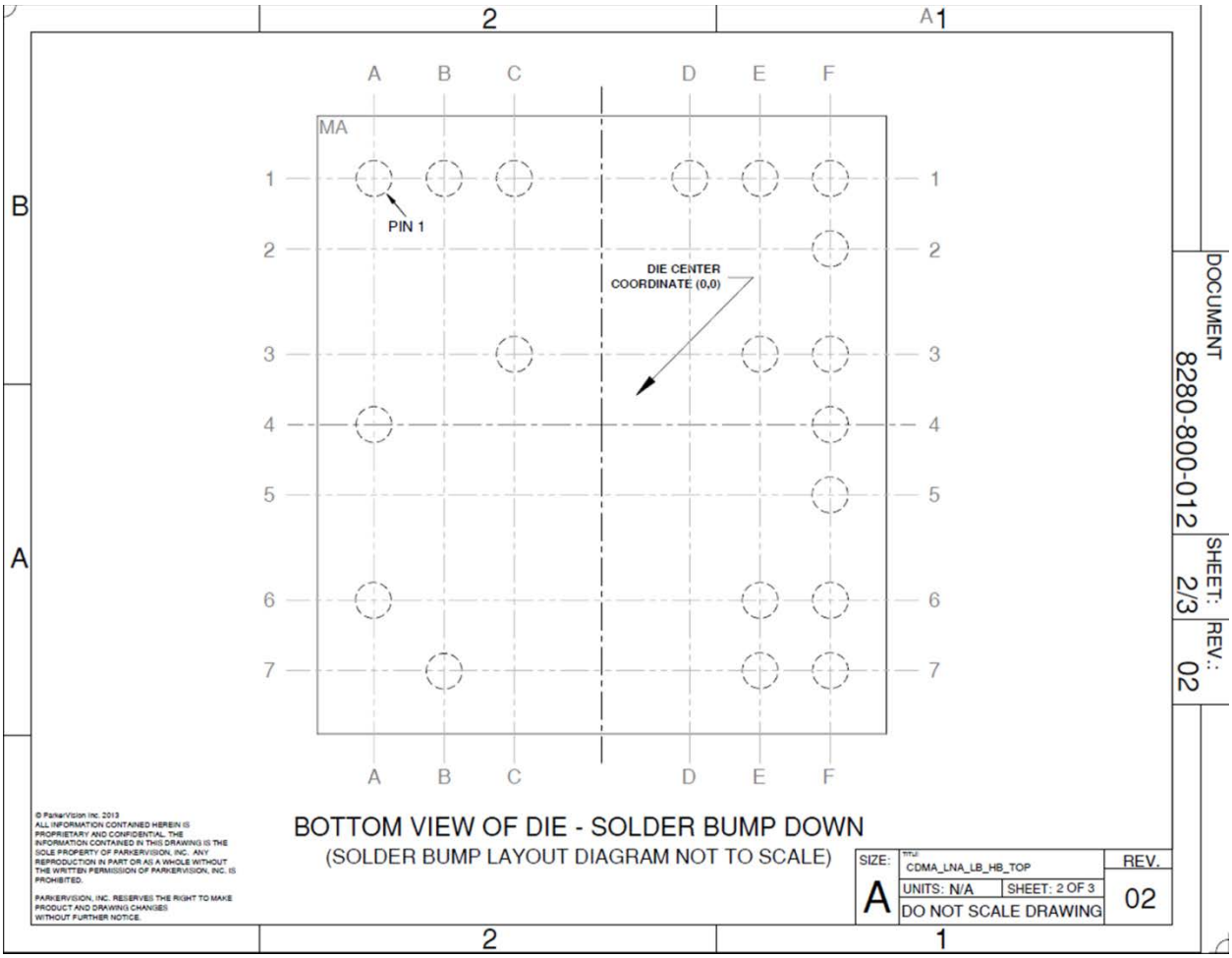
Bill of Materials – Evaluation Board

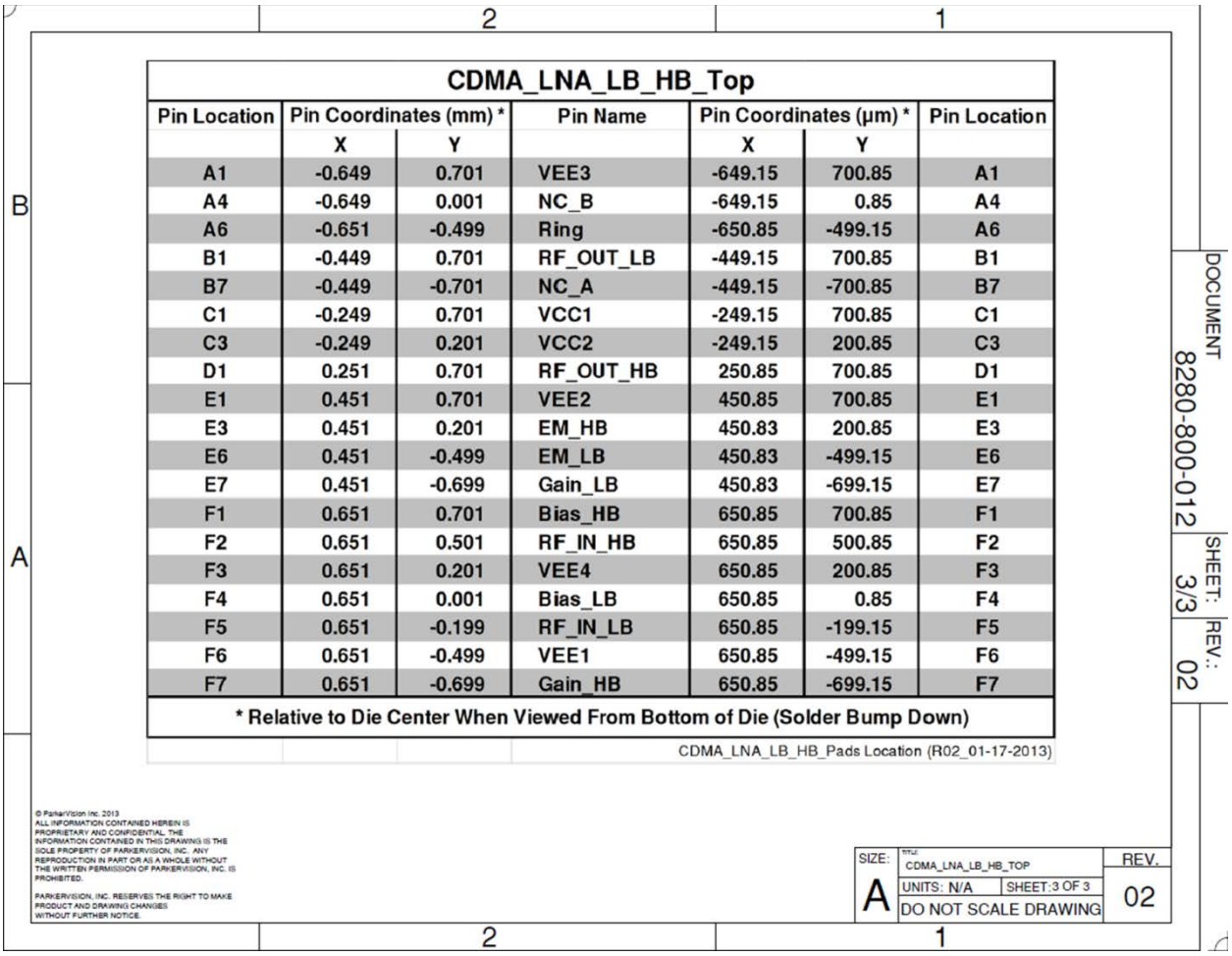
Item	Qty	Reference	Part Description	Part Number	Manufacturer
1	2	C2,C8	TBD	TBD	ATC
2	1	C3	10uF	TAJR106M006RNJ	AVX
3	3	C4,C13,C14	0.1uF	GRM155R71A104KA01J	Murata
4	1	C5	1000pF	GRM1885C1H102J	Murata
5	1	C6	56pF	GRM1885C1H560J	Murata
6	1	C9	3.3pF	600L3R3BT	ATC
7	1	C10	27pF	600L270JT	ATC 600 L
8	1	C12	8.2pF	600L8R2BT	ATC (600 L
9	4	J1,J3,J4,J5	SMA_E/L_0.062"	142-0701-801	Johnson
10	3	J2,J6,J7	HEADER 3	69190-403	Berg
11	1	L1	68nH	0402HP-68NX_L	Coilcraft
12	2	L2,L4	DNP	DNP	Coilcraft
13	1	L3	120nH	0402HP-R12NX_L	Coilcraft
14	1	L5	3.3nH	0402HP-3N3X_L	Coilcraft
15	1	L6	5.6nH	0402HP-5N6X_L	Coilcraft
16	1	L7	12nH	0402HP-12NX_L	Coilcraft
17	4	R1,R2,R4,R6	0	MCR01MRTJ000	Rohm
18	1	R3	499	MCR01MRTF4990	Rohm
19	1	R5	1k	MCR01MRTJ102	Rohm
20	2	R7,R8	100k	MCR01MRTJ104	Rohm
21	1	U1	PVL2520R	PVL2520R	ParkerVision

Mechanical Information

Dimensions and Pad Locations







CDMA_LNA_LB_HB_Top						
Pin Location	Pin Coordinates (mm) *		Pin Name	Pin Coordinates (µm) *		Pin Location
	X	Y		X	Y	
A1	-0.649	0.701	VEE3	-649.15	700.85	A1
A4	-0.649	0.001	NC_B	-649.15	0.85	A4
A6	-0.651	-0.499	Ring	-650.85	-499.15	A6
B1	-0.449	0.701	RF_OUT_LB	-449.15	700.85	B1
B7	-0.449	-0.701	NC_A	-449.15	-700.85	B7
C1	-0.249	0.701	VCC1	-249.15	700.85	C1
C3	-0.249	0.201	VCC2	-249.15	200.85	C3
D1	0.251	0.701	RF_OUT_HB	250.85	700.85	D1
E1	0.451	0.701	VEE2	450.85	700.85	E1
E3	0.451	0.201	EM_HB	450.83	200.85	E3
E6	0.451	-0.499	EM_LB	450.83	-499.15	E6
E7	0.451	-0.699	Gain_LB	450.83	-699.15	E7
F1	0.651	0.701	Bias_HB	650.85	700.85	F1
F2	0.651	0.501	RF_IN_HB	650.85	500.85	F2
F3	0.651	0.201	VEE4	650.85	200.85	F3
F4	0.651	0.001	Bias_LB	650.85	0.85	F4
F5	0.651	-0.199	RF_IN_LB	650.85	-199.15	F5
F6	0.651	-0.499	VEE1	650.85	-499.15	F6
F7	0.651	-0.699	Gain_HB	650.85	-699.15	F7
* Relative to Die Center When Viewed From Bottom of Die (Solder Bump Down)						

CDMA_LNA_LB_HB_Pads Location (R02_01-17-2013)

DOCUMENT 8280-800-012 | SHEET: 3/3 | REV.: 02

SIZE: A | TITLE: CDMA_LNA_LB_HB_TOP | REV. 02 | UNITS: N/A | SHEET:3 OF 3 | DO NOT SCALE DRAWING

Die Image