PV2510P-1A

Digitally Controlled Power Supply (DCPS)

The PV2510P is a highly efficient, digitally controlled switching power supply, capable of sourcing up to 1A of continuous current and peak currents of 2A. The PV2510P is optimally designed to target 3G and 4G applications, providing excellent regulation and efficiency over the full output dynamic range. The power supply output voltage is digitally programmable from 0.6 to 4.0V in steps of 54mV through an SPI interface, with an output voltage settling time of less than 50µs for full scale output changes.

General Features

- Battery Input Voltage: 3.0V to 4.3V
- 1.0A Continuous / 2.0A Peak Output Current
- Up to 97% Efficient
- Programmable Output Voltage: 0.6 to 4.0V
  - 6 bit resolution, 54mV steps
- < 50µs Settling Time (full scale voltage Δ)
- Programmable Bypass Mode
- Programmable Clock Dither Mode
- Low Current Power Down Mode ~ 10µA
- 16-pin QFN package (3.0x3.0mm) or Wafer Scale Package
- Temp range: -40 to +85°C

Primary Applications

- Handheld Electronics
- Mobile Phones
- Portable Computers
- Test Equipment

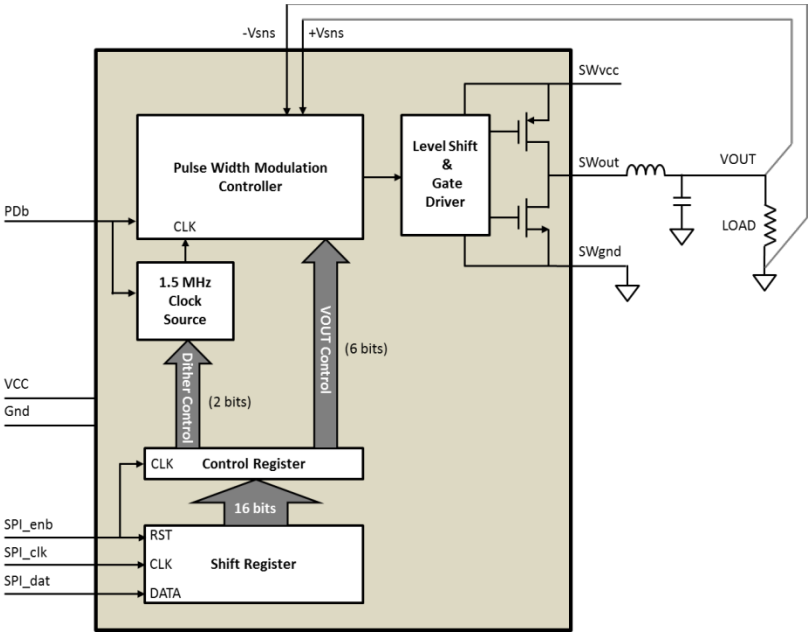

Figure 1: PV2510P Functional Block Diagram

Contents

Pin Description

Table 1: Pin Description

Pin Number	Pin Name	Description
1	SWvcc	Regulator input supply voltage (up to 2A)
2	SWgnd	Regulator input supply ground (up to 2A)
3	SPI_enb	Serial interface enable. When this pin is low the SPI is active *(Internal Pull-Up Circuit)*
4	SPI_clk	Serial interface clock *(Internal Pull-Down)*
5	SPI_dat	Serial interface data *(Internal Pull-Down)*
6	Vcc	Interface and control supply voltage
7	Gnd	Interface and control supply ground
8	PDb	Power down input. When low, the chip is powered down, except for SPI. *(Internal Pull-Down)*
9	+Vsns	Positive voltage sense input
10	-Vsns	Negative voltage sense input
11	SWgnd	Regulator input supply ground (up to 2A)
12	SWvcc	Regulator input supply voltage (up to 2A)
13	SWout	Regulator output to the external inductor
14	SWout	Regulator output to the external inductor
15	SWout	Regulator output to the external inductor
16	SWout	Regulator output to the external inductor
17	EPAD	Exposed pad underneath package

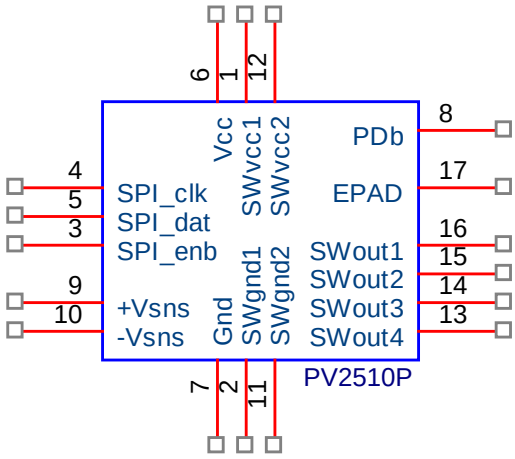

Figure 2: Pin Connection Diagram

Electrical Specifications

(Package: -40°C to +85°C, Junction: -40°C to +100°C)

Parameter	Conditions	Min	Typ	Max	Unit
Switch Supply Voltage (SWvcc)		3.0		4.3	V
Control supply Voltage (Vcc)		2.7	3.0	3.6	V
Control supply current			3	5	mA
Current in Power Down Mode	Switch Supply leakage		10		µA
	Control Supply leakage[1]			1	µA
Logic "High" Voltage		1.7		Vcc+0.3	V
Logic "Low" Voltage		Gnd-		0.7	V
Output Voltage	Variable	0.60		4	V
Drop out	Input voltage – Output voltage			0.3	V
Output Voltage Resolution	Variable in Increments		54		mV
PMOS Switch on resistance			0.20	0.35	Ω
NMOS Switch on resistance			0.20	0.35	Ω
Output inductor			4.7		µH
Output capacitor	Suggested for ripple < 5mV		10		µF
Capacitor ESR	Suggested for ripple < 5mV		.025		Ω
Efficiency @ 4V Out	Input Voltage 4.3V, Load Current 0.1A to		95		%
Peak Current limit[2]	Regulator will limit forward currents to this level		2		A
Switching Frequency		1		2	MHz
Dither pattern length		256	1500		cycles
Dither magnitude (Max. frequency change for dither)	Dither magnitude cntl bit =0	-20		+20	%
	Dither magnitude cntl bit =1	-40		+40	%
Dither frequency steps	Total number of discrete frequencies for		32		steps
Absolute Output Voltage Accuracy Vout > 1V	Iout=0A<Iout<1A SWvcc=+3.0V to +4.3V	-5		5	%
Absolute Output Voltage Accuracy Vout < 1V	Iout=0A<Iout<1A SWvcc=+3.0V to +4.3V	-50		50	mV
Line Regulation	SWvcc = +3.0V to +4.3V		3		mV/V
Load Regulation	Iout = 100mA to 1A		7		mV/A
Start Up Time	Rising edge of PDb input to when absolute voltage accuracy is met			50	µs
Voltage step time	Time to step voltage levels			50	µs
Maximum rate of current change	Maximum rate that will maintain the voltage spec.		10000		A/s

Note 1: Does not include pull-up and pull-down current from the digital inputs.

Note 2: The regulator will limit instantaneous currents in the forward direction but will not limit the negative current flow.

Application Information

Overview

The PV2510P is a synchronous, fixed frequency PWM, step-down (buck), DC-DC regulator having a dynamically programmable output voltage via an SPI interface. A typical application schematic is shown Figure 3, below.

The input/output voltage relationship of a buck regulator is controlled by the duty cycle (PWM) of the internal switch and is governed by the following relationship:

$$D = \frac{V_{out}}{V_{in}}$$

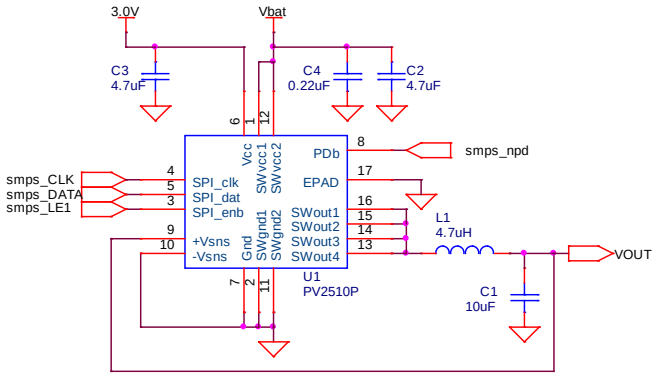

Figure 3: Typical Application Schematic

Selection of Output Inductor

The 4.7uH output power inductor chosen should possess as low a DCR as possible, to optimize efficiency, and a current rating that is sufficient for the given application. Either parameter competes with physical size of the component. To aid in the selection of current rating the peak inductor current is given by the following relationship:

$$I_{peak} = I_{out} + V_{out} \cdot \frac{\left(1 - \frac{V_{out}}{V_{in}}\right)}{2 \cdot f \cdot L}.$$

Selection of Output Capacitor

Regulator output ripple increases with capacitor ESR. As such, a low ESR ceramic capacitor is recommended with an X5R or X7R temperature rating.

Bypass Mode

When placed in bypass mode (SPI control), the large PWM switch remains closed, connecting the battery input (pins1 & 12) to the regulator output (pins 13 through 16). This is true even during power down mode (see Table 2).

Dither Mode

When placed in dither mode (SPI control), the switching frequency is modulated by a pseudo-random pattern, as a means of spreading clock spurious energy at the regulator output, reducing discrete spectral tones. The magnitude of the frequency dither can be chosen to be +/-20% or +/-40% of the clock frequency. Please note, that the average output voltage is still regulated to the desired level and accuracy while in dithering mode.

Power Down

When the PDb pin is pulled low, all blocks within the PV2510P are powered down, except for the SPI interface. The truth table in Table 2, below, shows the state of the regulator output in power down mode. Notice that even while powered down, setting the bypass bit high, will short the output to the regulator input. This feature enables a maximum efficiency bypass mode, as opposed to an "active" bypass mode.

Table 2: Regulator Output State in Power Down Mode

"bypass" Bit	"dsync" Bit	Regulator Output State
0	0	Output shorted to GND
0	1	Output Tri-Stated
1	X	Output shorted to Battery Input

Digital Inputs

There are four digital inputs on the PV2510P. Each input is designed to use a +3V power supply and accept +2.5V inputs.

Digital Inputs with Internal Pull-Down Circuits:

If left floating, these inputs will be pulled to ground through a 250k Ohm resistor. These inputs will draw no supply current if the input is less than ~0.2V. *For best operation these inputs should be driven low or allowed to pull low when not in use.*

Digital Inputs (Continued)

Digital Inputs with Internal Pull-Up Circuits:

If left floating these inputs will be pulled up to a voltage that causes the buffer's output to go high. Then the pull up resistor is disconnected and the input is allowed to float. This is done to minimize the supply current while in the 'high' state. This input will draw about 0.5uA when the input is greater than 1.7V. *For best operation this input should have an external pull up resistor to 2.5V to ensure the input is not accidentally triggered.*

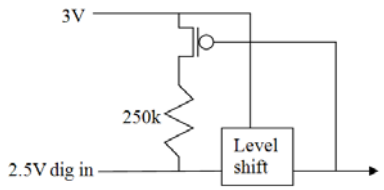

Figure 4: Simplified Pull-Up Input Circuit

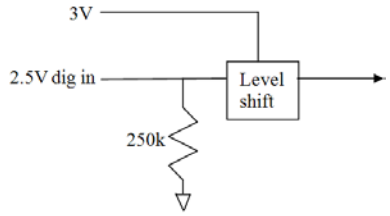

Figure 5: Simplified Pull Down Input Circuit

SPI Interface

The PV2510P is configured and controlled via an SPI interface, using a single 16 bit word. The SPI interface remains operational, even while the device is in power down mode. This feature facilitates configuring the device while powered down, so if desired, the device is already properly configured when returned to normal, operation. Moreover, since the clock on the SPI_clk input pin may be stopped between SPI transactions, current in power down mode remains very low.

The SPI interface on the PV2510P is write-only, and has no read-back capability. Referring to the timing diagram in Figure 6, below, it can be seen that an SPI write transaction begins by asserting the SPI_enb pin low on the device. Once low, the 16 bit serial data is then shifted in on the rising edge of SPI_clk, MSB first. Upon shifting in all 16 bits, the SPI_enb signal is then de-asserted (high), ending the SPI transaction.

The new 16 bit word is clocked into the control register from the input shift register on the rising edge of the SPI_enb signal. As a result, the new control word takes effect upon the rising edge of the SPI_enb signal. Conversely, the input shift register is reset to its default state when the SPI_enb signal is low. Consequently, the PV2510P may be put into its default configuration by cycling the SPI_enb signal high-low-high.

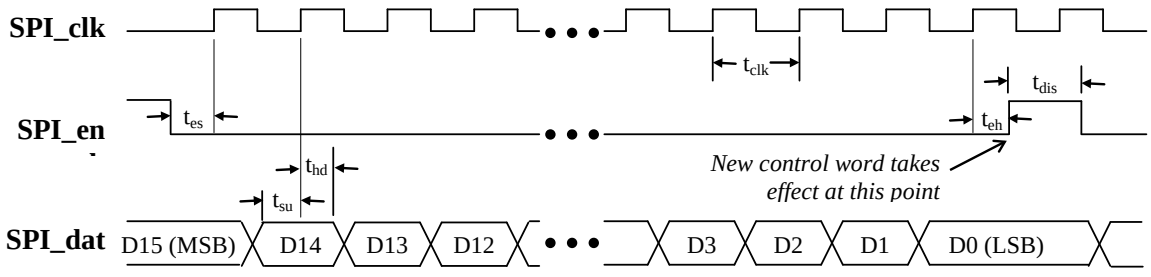

Figure 6: SPI Timing Diagram

Table 3: SPI Interface Timing Specifications

Parameter	Description	Min	Max	Units	Comments
tclk	Clock period	20		ns	50% duty cycle
tsu	Data setup time	10		ns	
thd	Data hold time	10		ns	
tes	Enable setup time	10		ns	
teh	Enable hold time	10		ns	
tdis	Disable time	20		ns	
Vhi	High input voltage	1.7	Vcc+0.3	V	CMOS levels relative to the control supply voltage
Vlo	Low input voltage	Gnd-0.3	0.7	V	

Table 4: Control Register Map

Bit #	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Field	ilp[2]	ilp[1]	ilp[0]	olp[2]	olp[1]	olp[0]	dsync	dmag	dthr	byps	V[5]	V[4]	V[3]	V[2]	V[1]	V[0]
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5: Control Register Fields & Description

Field	Name	Description
V[5:0]	Voltage Control	This 6 bit word sets the regulator output voltage. The output voltage is given by the following equation: ***VOUT = 0.60 + V[5:0]*(3.4/63)*** where V[5] is the MSB of the voltage control field.
byps	Bypass Enable	Regardless of the state of the PDb input pin (power-down input), when this bit is high, the regulator will stop switching and short the regulator output (pins 13 through 16) to the input supply (pins1 & 12). When this bit is low the regulator will operate normally.
dthr	Dither Enable	When this bit is high, the switching oscillator frequency will be dithered by modulating the switching frequency with a pseudorandom pattern. When this bit is low, the switching frequency will be fixed at the nominal frequency.
dmag	Dither Magnitude	This bit controls the magnitude of the frequency dither when dither is enabled (*dthr* = 1). When this bit is low, the frequency is changed a maximum of ±20%, when this bit is high, the frequency is changed a maximum of ±40%. Setting the dither magnitude to the larger value may reduce the peak spur at the output, but will generate noise over a wider bandwidth.
dsync	Disable Synchronization	This bit allows the user to configure the regulator as a traditional, non-synchronous, buck regulator. When this bit is high, the synchronous switch to ground will be fixed in the open position. If a diode is connected between the output and ground while this bit is high, the regulator will operate as a non-synchronous buck regulator. This option could provide improved efficiency at low output currents, but will not be as efficient at high output currents. When this bit is low the regulator operates normally.
olp[2:0]	Outer Loop Gain	This 3 bit field controls the voltage comparator gains in the outer control loop. These gains can be adjusted to optimize the stability and performance when using other than the recommended output L and C values. (See Table 6)
Ilp[2:0]	Inner Loop Gain	This 3 bit field controls the current gain and compensation of the inner control loop. These gains can be adjusted to optimize the stability and performance when using other than the recommended output L and C values. (See Table 7)

Table 6: Outer Loop Gain Settings

olp value	Outer Loop Gain Settings
0 (000)	All gains nominal
1 (001)	Integrator gain nominal, linear gain –50%
2 (010)	Integrator gain nominal, linear gain +50%
3 (011)	Integrator gain –50%, linear gain +50%
4 (100)	Integrator gain +50%, linear gain nominal
5 (101)	Integrator gain +50%, linear gain –50%
6 (110)	Integrator gain +50%, linear gain +50%
7 (111)	Integrator gain –50%, linear gain –50%

Table 7: Inner Loop Gain Settings

ilp value	Inner Loop Gain Settings
0 (000)	All gains nominal
1 (001)	Current mode compensation nominal, DC gain -40%
2 (010)	Current mode compensation nominal, DC gain +60%
3 (011)	Current mode compensation nominal, DC gain +25%
4 (100)	Current mode compensation +30%, DC gain nominal
5 (101)	Current mode compensation +30%, DC gain –40%
6 (110)	Current mode compensation +30%, DC gain +60%
7 (111)	Current mode compensation +30%, DC gain +25%

Typical Performance Plots

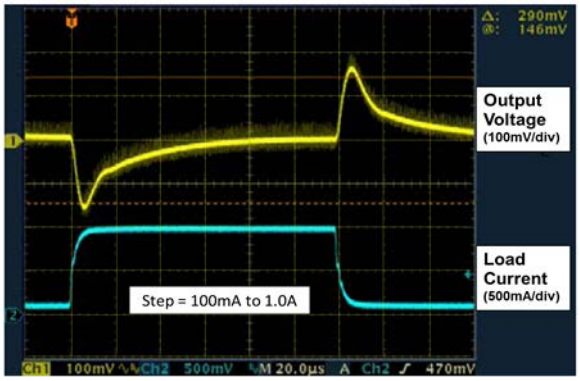

Figure 7: Load Step Response @ VOUT=1.8V

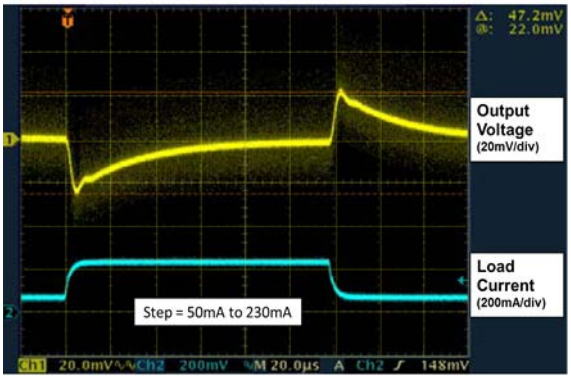

Figure 8: Load Step Response @ VOUT=1.8V

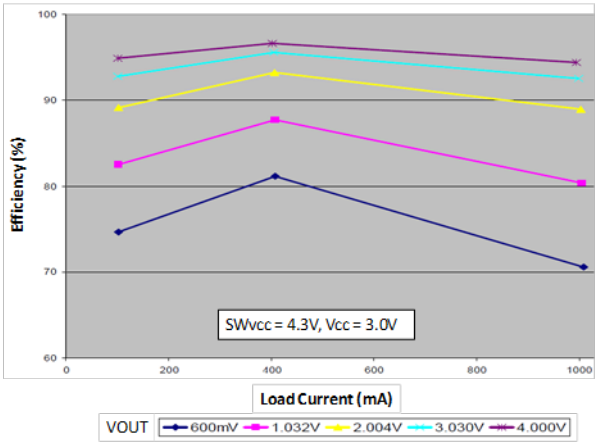

Figure 9: Efficiency vs. Load Current & VOUT

Mechanical Information

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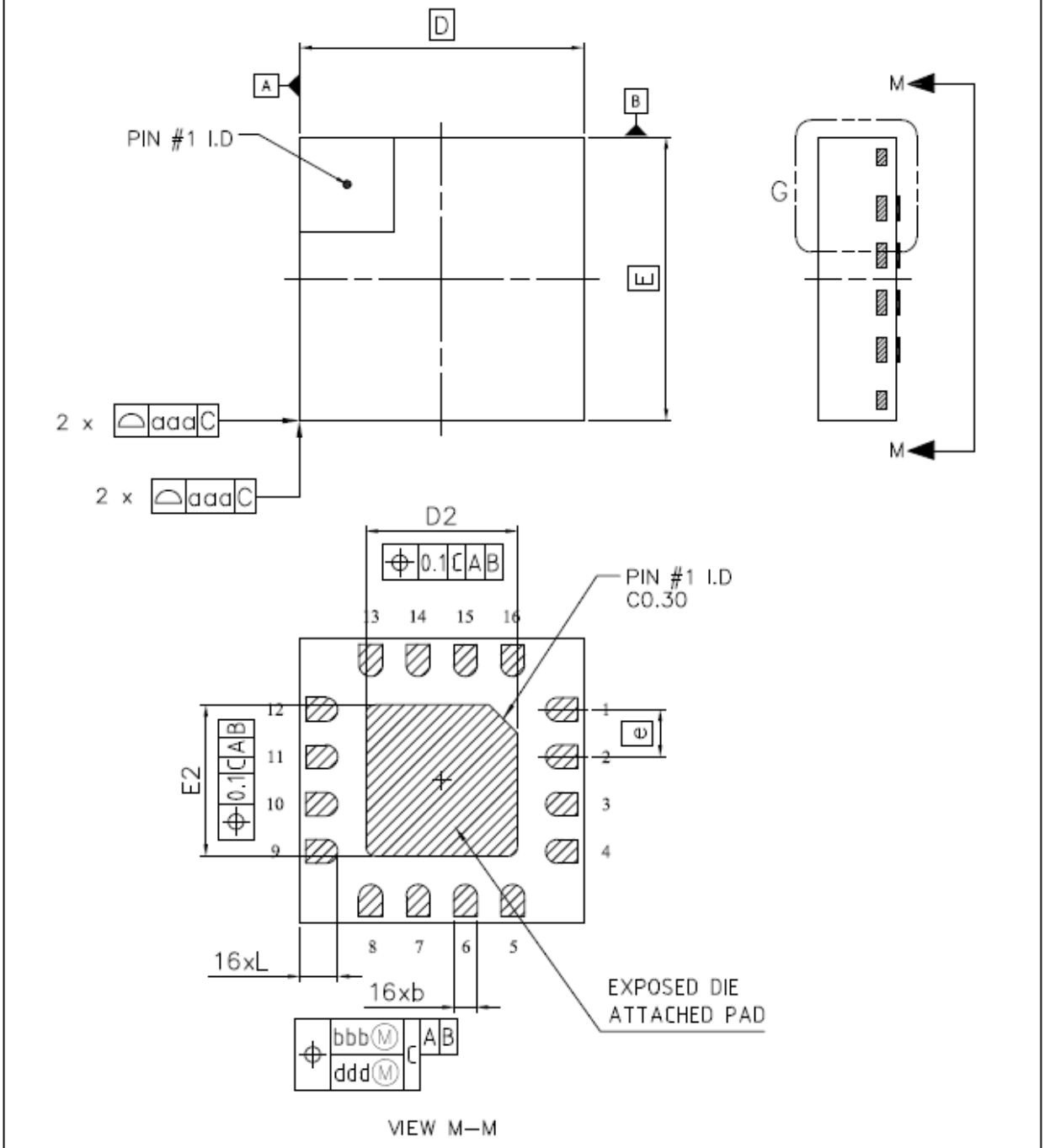
		ISSUE	O
		DATE	JUL.31,2008



TITLE: QFN 3X3 16LD 1.90 X 1.90mm PAD	COMPANY	*ASE KOREA*
	SHEET	1 OF 3

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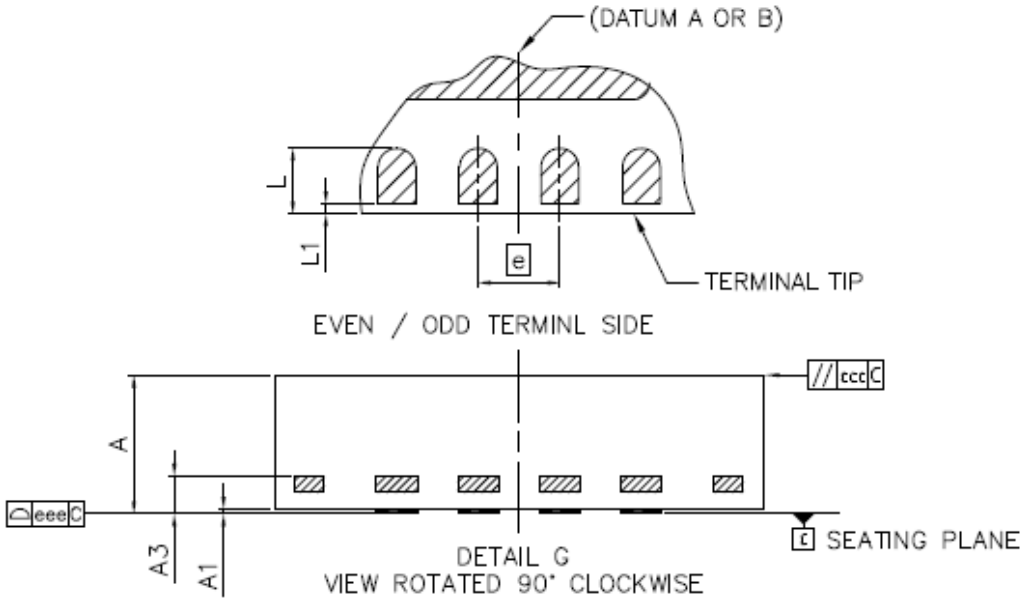
		ISSUE	O
		DATE	JUL.31,2008



DIM	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00		0.05
A3		0.203 REF	
b	0.20	0.25	0.30
D		3.00 BSC	
E		3.00 BSC	
D2	1.50	1.60	1.70
E2	1.50	1.60	1.70
e		0.50 BSC	
L	0.35	0.40	0.45
L1	0.00		0.10
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

NOTES

1.0 DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.

2.0 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

3.0 DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP. DIMENSION L1 REPRESENTS TERMINAL FULL BACK FROM PACKAGE EDGE UP TO 0.1mm IS ACCEPTABLE.

4.0 COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.

5.0 RADIUS ON TERMINAL IS OPTIONAL.

TITLE:		COMPANY	*ASE KOREA*
QFN 3X3 16LD 1.90 X 1.90mm PAD		SHEET	2 OF 3

ASE Advanced Semiconductor Engineering Korea, Inc.	PACKAGE OUTLINE	DWG NO.	98SPP16077A
		ISSUE	O
		DATE	JUL.31,2008

REVISION HISTORY ;

REV	DESCRIPTION	PREPARED BY	REVIEWED BY
O	Initial issue	H.J.Han/Jul.31,2008	S.K.Kang/Jul.31,2008

TITLE: QFN 3X3 16LD 1.90 X 1.90mm PAD	COMPANY	ASE KOREA
	SHEET	3 OF 3